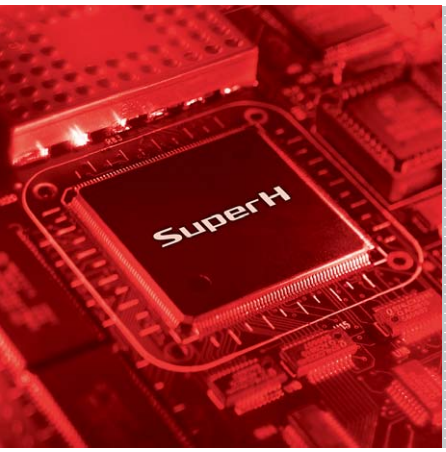


# SuperH® Family of Microcontrollers and Microprocessors

2007.4

Everywhere you imagine.

# Renesas Technology America

## SuperH® Family of Microcontrollers & Microprocessors **2007 Catalog**


- **One of the world's leading ITDM (Integrated Device and Technology Manufacturer) companies serving the global market**
- **In-house manufacturing capability for advanced process nodes –90, 65 and 45 nm**
- **Complete System-Level Solutions —** Solutions in all core segments (automotive, mobile, consumer, industrial and PCs) with the right mix of technology such as networking (wired/wireless), security, low power and analog/RF interface capabilities; plus full-scale development support
- **Proven credibility based on more than 30 years of experience**
  - — "Zero Defects" as the objective
  - — Compliance with international standards such as ISO/TS 16949
  - — High quality tested and proven by customers
  - — Commitment to safety and protection of environment

## Renesas — Your Best Decision for Microcontrollers and Microprocessors

*Choose for your next design; use for all your future ones.*

Renesas Technology, the #1 global supplier of microcontrollers, offers hundreds of devices in our M16C™, H8®, and SuperH® families, among others, that have solid technology roadmaps and cover wide spans of performance, integration, power efficiency and price points. Our advanced silicon solutions simplify system optimizations, facilitate design enhancements and diversifications, and help you meet tight cost budgets. You can shorten your system design cycles and improve your time-to-market by taking advantage of our total system support, which includes starter kits, HW/SW tools, reference designs/platforms, example software code, and middleware. Expert third-party support is available as well.

lead·FREE

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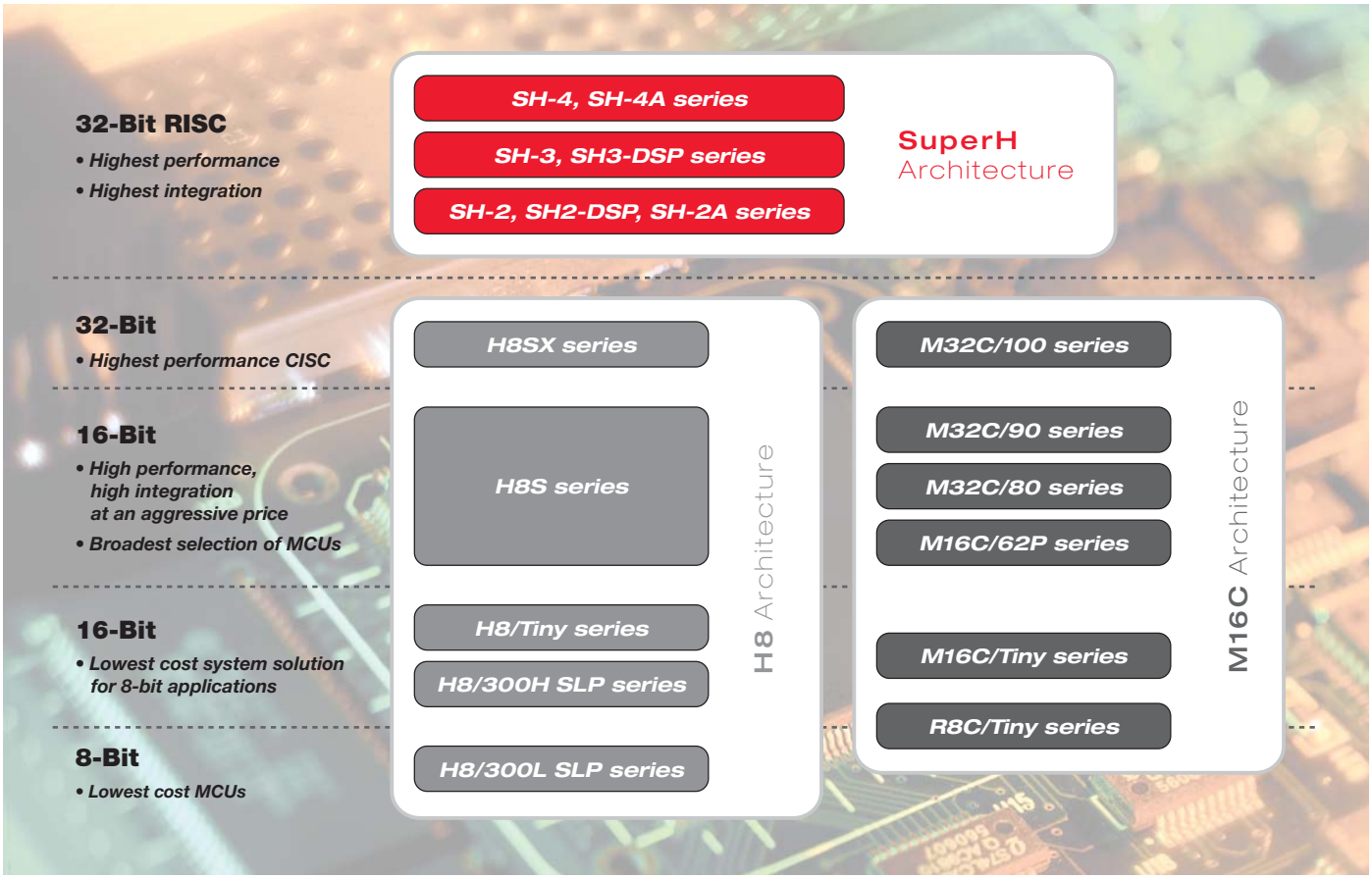
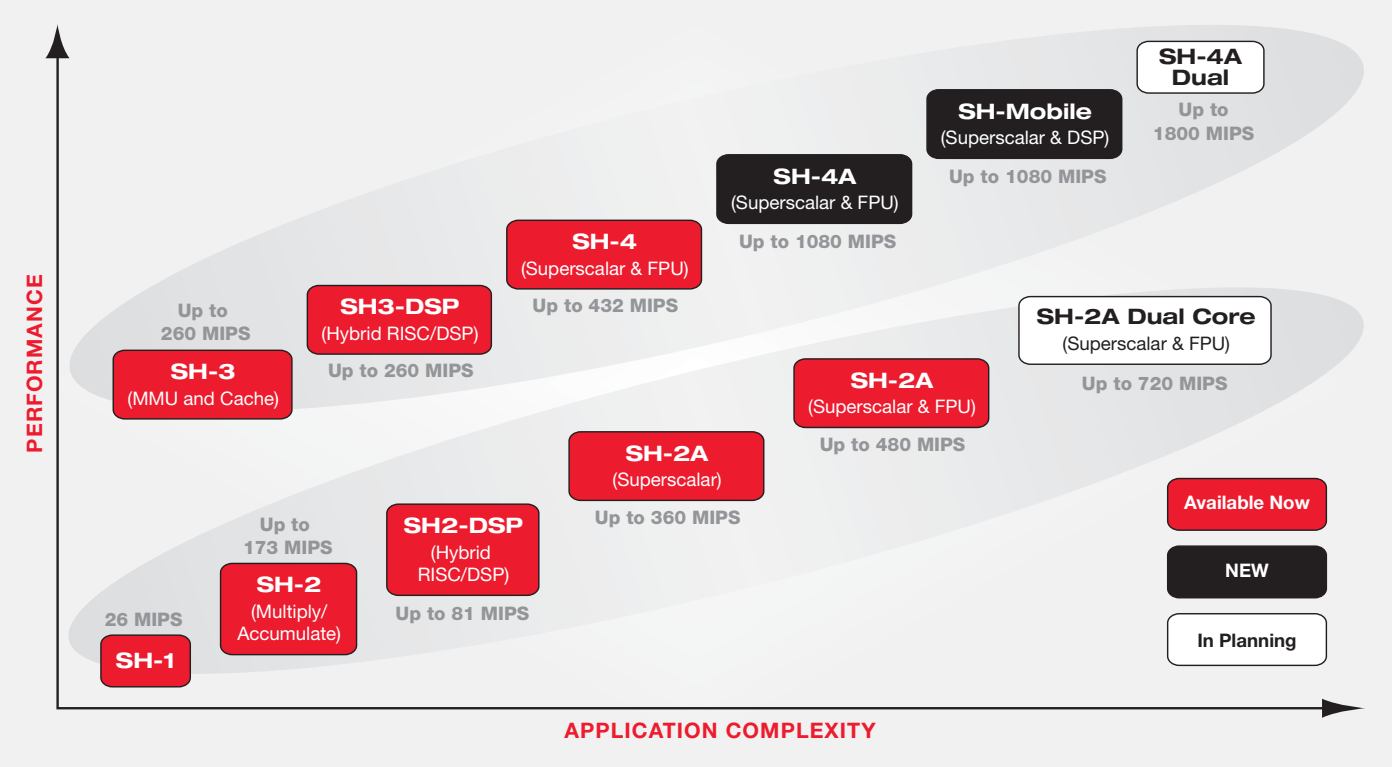



| Market Needs | SuperH Solutions |
|---|---|
| Performance | Up to 1080 MIPS, 4.2 GFLOPS (SH-4A); up to 360 MIPS (SH-2A), superscalar architecture |
| Cost/performance | High MIPS/$ ratings |
| Power/performance | High MIPS/W ratings |
| Code efficiency | 16-bit instructions: up to 40% smaller memory footprint, up to 40% more data in cache |
| Flash ROM | Up to 1MB flash, accessible in one cycle at 80MHz; single-voltage programmable |
| Floating-point and DSP support | DSP (SH2-DSP, SH3-DSP), superscalar FPU (SH-2A, SH-4, SH-4A), Superscalar DSP (SH-Mobile) |
| Graphics support | Superscalar operation [FPU operations independent of non-FPU operations] (SH-2A, SH-4, SH-4A) 2D and 3D graphics engine (SH-Mobile) |
| Video and Imaging | H.264, MPEG4, H.263, and JPEG engines |
| On-chip peripherals | Timers, DSP, MMU, A/D, D/A, memory controller, LCD controller, AFE, motor controller, cache, BSC, crypto accelerator, more |
| Industry-standard interfaces | USB, Ethernet, PCI, SCI, $I^2C$, PCMCIA, SSI (Audio), CAN, Smart Card, IrDA, SDRAM, DDR-SDRAM, NAND flash, memory card, camera |
| Architecture roadmap | Instruction set accommodates superscalar designs |
| Code compatibility | Upward compatible families (SH-1, SH-2, SH-3, SH-4) |
| Power consumption | Low static/dynamic operating currents, high MIPS/W ratings, power-down modes |
| Development environment | Comprehensive integrated H/W and S/W tools, extensive third-party support, on-chip debug |
| Off-the-shelf solutions | Middleware, reference boards, broad OS support |
| Support and training | Experienced application engineers, online evaluation lab, training courses |

## The SuperH Family Roadmap




The first 32-bit SuperH RISC device was introduced in 1993. In the years since, this popular product line has continuously grown and steadily evolved. Today it encompasses ten major product families, with more in development. They continue a solid technology roadmap of innovation fine-tuned to meet the changing needs of designers of embedded systems for diverse global markets.

A steadfast goal throughout the history of the SuperH family has been to produce microcomputers [microcontrollers (MCUs) and microprocessors (MPUs)] that deliver optimum mixes of performance and functionality, achieve requisite levels of performance at low power, and have compact packages. We also work to ensure that SuperH devices are offered at competitive prices and are supported by a comprehensive suite of Renesas hardware and software development tools. Importantly, we maintain code compatibility throughout the product line to facilitate software reuse that saves development time and engineering cost.

Renesas offers SuperH MCUs for general-purpose applications and SuperH MPUs for specialized applications. The MCUs in our SH-1, SH-2, SH2-DSP, and SH-2A series for general-purpose embedded system use offer CPU performance up to 480 MIPS and have reliable, high-capacity flash memory that is easy to use and simplifies system designs. The MPUs in our SH-3, SH3-DSP, SH-4, and SH-4A series for specialized applications deliver performance levels up to 1080 MIPS and provide on-chip peripherals tailored for leading-edge applications in automotive, mobile, and PC/AV markets, among others. Support for SuperH MCUs and MPUs is comprehensive, encompassing development tools, operating systems, drivers, middleware, and other products and services from Renesas and a large international community of technology partners and third-party vendors. This support facilitates the rapid development of SuperH-based products and solutions.

Renesas SH-Mobile application processors are used in tens of millions of mobile phones for offloading the processing of multimedia content from the main CPU. This baseband-independent design approach facilitates the rapid evolution of cell phones and other portable devices that can handle innovative new communication services and features without impacting the implementation of proven protocol processing methods. Beyond those markets, highly versatile SH-Mobile devices suit an expanding array of products that require smooth audio/video capture and playback, fast processing for software stacks, flexible connectivity options, and small form factors.

SH-Mobile devices perform master or co-processor roles, or both. All have powerful superscalar SH4A-DSP cores that readily handle JPEG, MPEG-1 Audio Layer 3 (MP3), and MPEG-4 data. The chips also provide extensive peripheral functions. For example, a built-in H.264 video engine achieves a 200% performance increase on average for most middleware, allowing reductions in CPU speed and power consumption.

Renesas supports SH-Mobile multimedia application processors with system development platforms, HW/SW tools and other resources. Additionally, the 200+ members of the SH-Mobile Consortium from around the world offer middleware, operating systems, board support packages, system integration assistance, and application support. Their technologies and services help speed time-to-market for complete system designs.

The SuperH family of MCUs and MPUs serve a wide range of embedded systems. The table on the next page summarizes key applications of each device series.

## SuperH Series Performance, Features and Applications

| Core | CPU/Bus Speed | Performance | Series | Features / Remarks | Key Applications |
|---|---|---|---|---|---|
| SH-2 | 80/40MHz | 104 MIPS | SH7080<br>SH7040<br>SH7140 | High-performance embedded controller with integrated RAM/cache/ROM/flash and advanced motor control timers | AC/DC drives, inverters, servo/motion controllers, machine tools |
| | 50/40MHz | 65 MIPS | SH7125 | SH/Tiny series; compact package | |
| | 133/66MHz | 173 MIPS | SH7600 | SH-Ether series; integrated Ethernet, host interface | Industrial control, networking |
| SH2-DSP | 62.5/31.25MHz | 81 MIPS/<br>125 MOPS | SH7065<br>SH7600 | Combined RISC/DSP architecture; derivatives with integrated Ethernet and PWM timers | Industrial control, networking, office automation |
| SH-2A | 200/66MHz | 480 MIPS | SH7200 | High performance, superscalar, optional FPU, fast interrupt response time | Industrial control, office automation, multimedia |
| SH-3 | 200/66MHz | 260 MIPS | SH7700 | Low-power consumption, high-speed, MMU, cache, SDRAM I/F, PCMCIA | Office appliances, bar code scanners, digital still cameras |
| SH3-DSP | 200/66MHz | 260 MIPS/<br>400 MOPS | SH7729R<br>SH7727<br>SH7720<br>SH7710 | Combined RISC/DSP architecture; pin-compatible to some SH-3 derivatives, other features similar to SH-3 devices | Handheld/portable devices, routers, cable modems, postage meters, multimedia, web phones |
| SH-4 | 240/120MHz | 432 MIPS<br>1.7 GFLOPS | SH7750R<br>SH7751R<br>SH7760 | High performance, superscalar, FPU, vector graphic operations, MMU, SDRAM I/F, PCMCIA, etc. | CIS/Telematics, video game consoles, sub-note books, set-top boxes, residential gateways, etc. |
| SH-4A | 600/300MHz | 1080 MIPS<br>4.2GFLOPS | SH7780<br>SH7785<br>SH7763 | High performance, superscalar, FPU, vector graphic operations, SuperHyway bus, MMU, DDR-SDRAM interface | CIS/Telematics, home multimedia, entertainment, gateways |
| SH4A-DSP | 400/133MHz | 720 MIPS<br>800 MOPS | SH-Mobile | High-performance, superscalar, DSP, video/imaging/graphics engines, SuperHyway bus, MMU | Portable multimedia players, digital TV, video phones, IP cameras |

## A Global Leading Position

Renesas Technology has acquired an impressive reputation for leadership and earned a large share of the embedded processor market in leading-edge growth areas of automotive and mobile applications. For example, through SuperH devices incorporating an SH-4 or SH-4A CPU core, we have gained about an 80% worldwide share of the microcontrollers used in car navigation systems. And our SH-Mobile family is the de facto standard in application processors for mobile phones, being used in over 200 different models. As we expand the SuperH family, we are applying the advanced technology acquired in those fields together with Renesas' long-term commitment for product availability to other markets that have technology and application challenges, such as industrial control and office automation. Techniques for obtaining improved power efficiency have wide appeal, as do on-chip peripherals and high code density. The SuperH family of MCUs and MPUs continues to be the architecture of choice for embedded system designers.

## SuperH Architecture: Common Features

### RISC-type instruction set

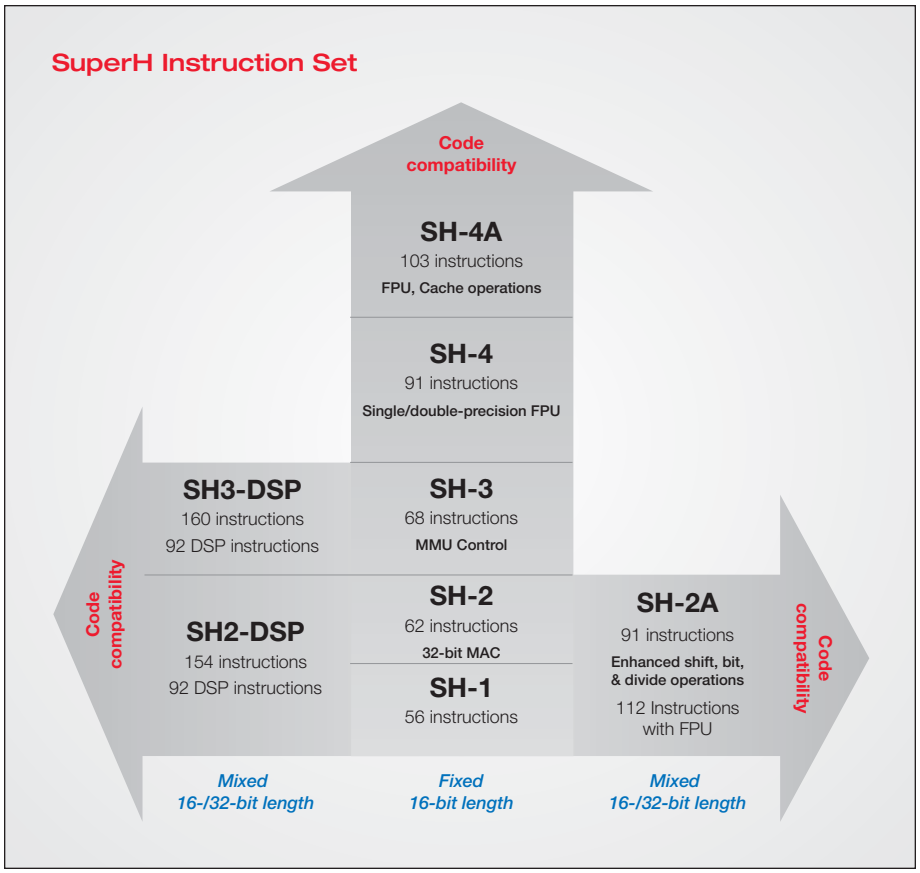
- Instruction length: fixed 16-bit-long instructions for improved code efficiency
- Load-store architecture (basic arithmetic and logic operations are carried out between registers)
- Delayed unconditional branch instructions reduce pipeline disruption
- Instruction set optimized for the C language

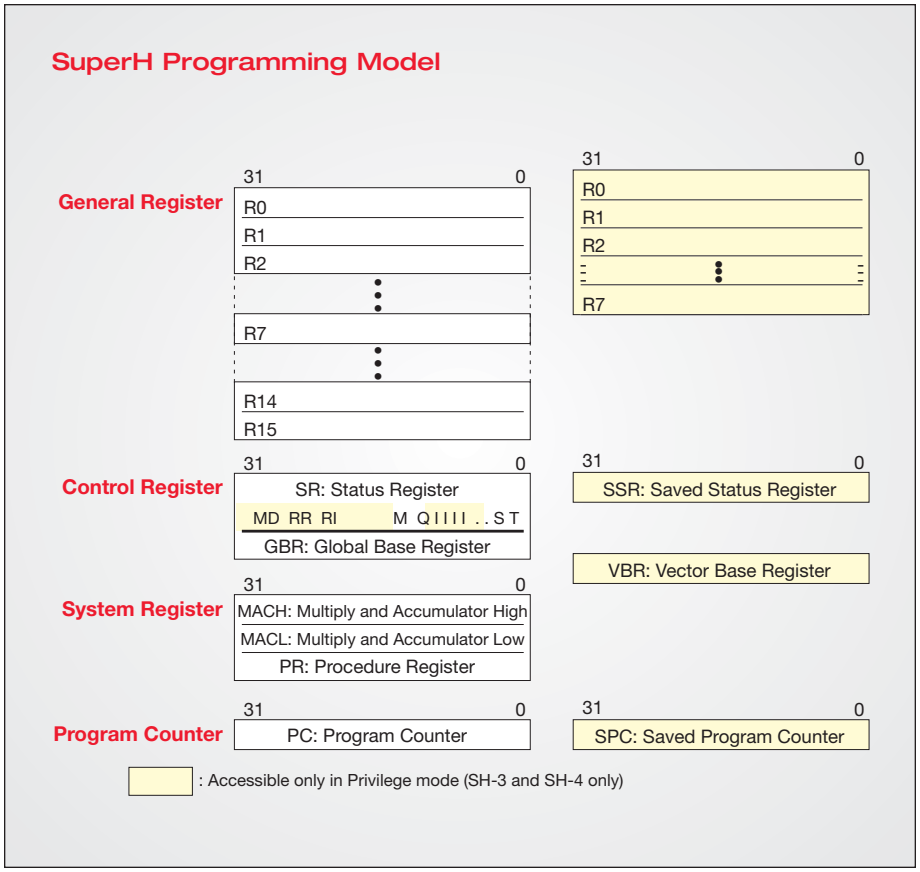
### CPU register set

- Sixteen 32-bit general-purpose registers
- Up to 7 control registers and 4 system registers for fast jumps and interrupt response

### Efficient caching scheme for each series

- LRU replacement policy algorithm for improved hit rates
- Each family's cache architecture has been optimized for the best latency/miss-rate balance: e.g., SH-4A devices have 32KB + 32KB, 4-way set-associative, separate instruction and operand caches for improved performance



## Built in hardware multiply-accumulate unit

- 16-bit x 16-bit + 42-bit (SH-1 devices)
- 32-bit x 32-bit + 64-bit (SH-2, SH-3, SH-4 chips)

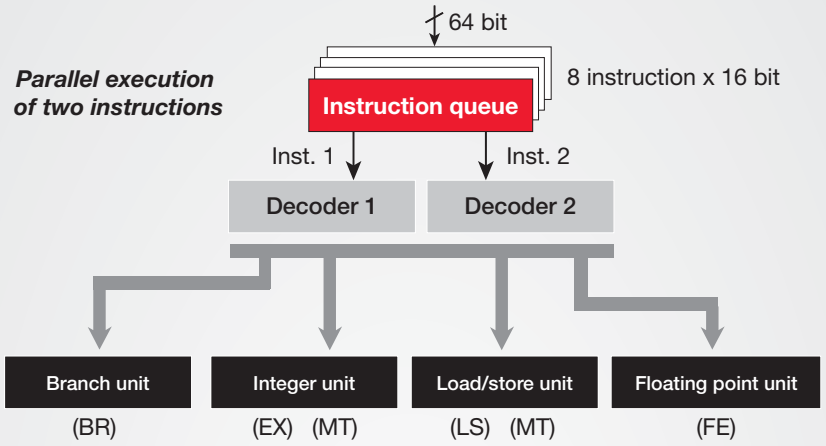
## Instruction execution

- Scalar architecture: One instruction per clock cycle
- Superscalar architecture (SH-2A/SH-4/SH-4A onwards): Maximum of two instructions per cycle
- 5-stage instruction pipeline (7-stage in SH-4A)

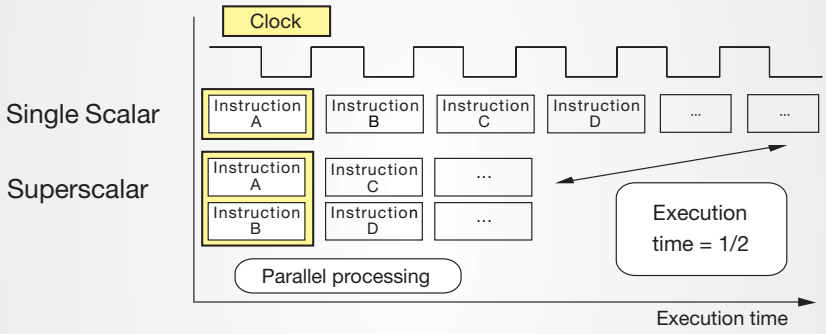
## Memory Management Unit for RTOS (SH-3 and beyond)

- 4-Gbyte address space, 256 address space identifiers (8-bit ASIDs)
- Single virtual mode and multiple virtual memory mode
- Supports multiple page sizes: 1KB, 4KB, 64KB, 1MB
- 4-entry fully-associative TLB for instructions
- 64-entry fully-associative TLB for instructions and operands
- Supports software-controlled replacement and random-counter replacement algorithm
- TLB contents can be accessed directly by address mapping

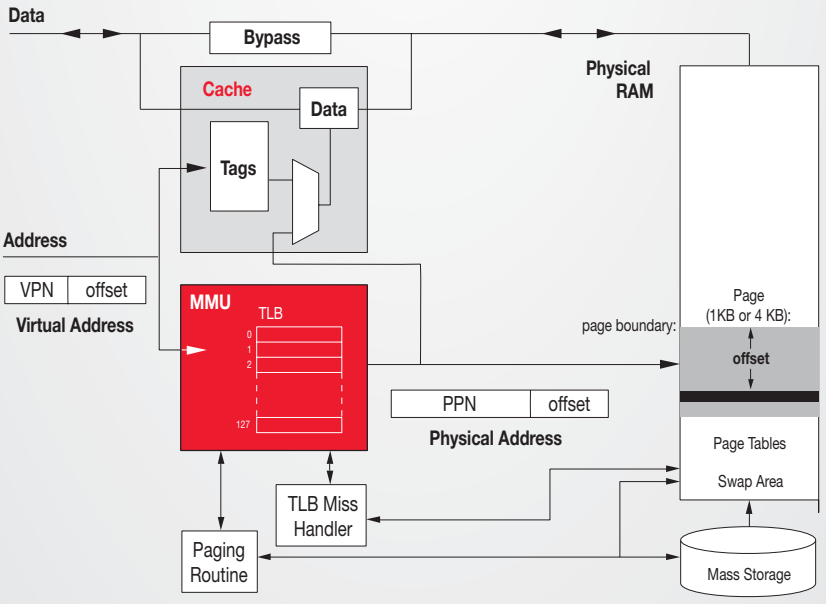
## SH-2A/SH-4/SH-4A Two-Way Superscalar Architecture




## Superscalar Operations




## MMU Block Diagram



## SH-2A Family Features

### Instruction set upward compatible with SuperH RISC Family

- Upward compatible with SH-1 and SH-2 Family of devices
- Compact 16/32-bit instruction code
- Flexible addressing modes.

### Integrated SH-2A CPU engine and FPU optimized for performance, low power and cost

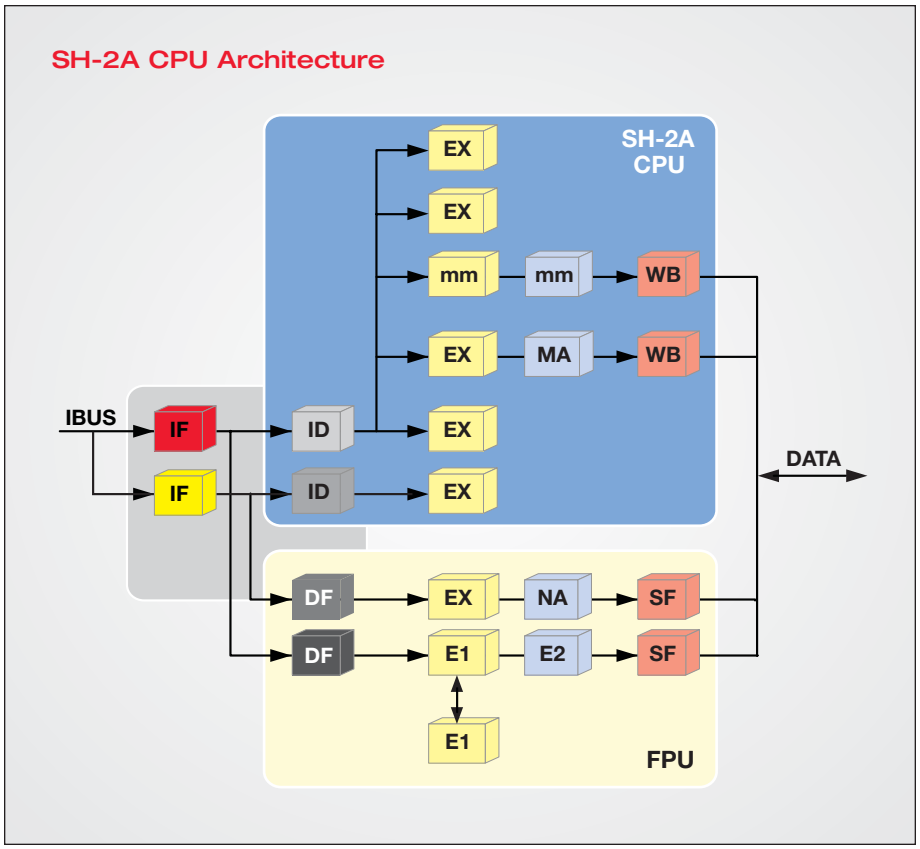
- Improved performance
  - 1.5x performance compared to SH-2 architecture
- Better code density
  - 75% code-size reduction compared to SH-2 core
- Real-time control
  - 6-cycle interrupt-response time
- Floating Point Unit (FPU):
  - 1.4 GFlops performance

### SH-2A CPU Architecture

- Superscalar RISC engine
- 32-bit Harvard architecture
- 5-stage RISC CPU pipeline
- Instruction/Data cache
- 2-instruction/cycle execution time
- Conditional delayed branching
- Flexible addressing modes
- On-chip multiplier unit supports MAC operations
- Prioritized exception handling

### SH-2A FPU Architecture

- Supports IEEE-754 compliant data types and exceptions
- Independent 5-stage pipeline
- Single/double-precision operation support
- 16 x 32-bit floating point registers
- Supports FMAC/FDIV/FMUL/FSQRT instructions




### Abundant Registers

- 16 x 32-bit general-purpose
  - R0 - R15
- 4 x 32-bit system registers
  - (MACH/L) High/Low Multiply & Accumulate registers
  - (PR) Procedure register
  - (PC) Program counter register
- 4 x 32-bit control registers
  - (SR) Status register
  - (GBR) Global base register
  - (VBR) Vector base register
  - (TBR) Jump-table base register
- 16 x 32-bit Floating Point Registers
  - FPR0 - FPR15
- Register banks
  - Allow contents of general registers R0 to R14, global register (GBR), the multiply and accumulate registers (MACH, MACL), the procedure register (PR), and the interrupt vector table address offsets (VTO) to be banked during interrupts

### Improved Instruction Set

- 16-bit basic instructions for improved efficiency
- 32-bit instructions for improved performance
- Delayed branch instructions.
- Register bank instructions for improved interrupt latency
- Barrel shift instructions supporting logical and arithmetic operations
- Multiple register save/restore instructions
- Instruction set based on C language for ease of development

### Easier to program; simplified product development

- Multitasking instead of multiprocessing
- Eliminates inter-processor communication
- Single hardware/software design environment

## SuperH On-Chip Floating Point Co-processor Architectural Features

- Supports single-precision (32 bits) and double-precision (64 bits)
- 10-stage floating instruction pipeline (SH-4A)
- Supports IEEE754-compliant data types and exceptions
- Floating-point registers: 32 bits x 16 words x 2 banks
- (Single-precision x 16 words, or double-precision x 8 words) x 2 banks
- 32-bit CPU-FPU floating-point communication register (FPUL)
- Supports FMAC (multiply-and-accumulate) instruction
- Supports FDIV (divide) and FSQRT (square root) instructions
- Supports FLDI0/FLDI1 (load constant 0/1) instructions
- 3D graphics instructions (single-precision only)
- 4-dimensional vector conversion and matrix operations (FTRV): 4 cycles (pitch), 8 cycles (latency)
- 4-dimensional vector (FIPR) inner product: 1 cycle (pitch), 5 cycles (latency)
- Instruction execution times
  - Latency (FMAC/FADD/FSUB/FMUL): 3 cycles (single-precision), 8 cycles (double-precision)
  - Pitch (FMAC/FADD/FSUB/FMUL): 1 cycle (single-precision), 6 cycles (double-precision)

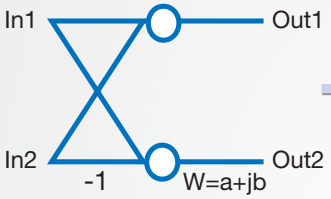
## 128-bit Floating Point Vector Engine: DSP/SIMD Instructions

16-tap, 40-sample block FIR (1.6 MACs/cycle)

***STAGE 1*** ... ***STAGE 4***

$$\begin{bmatrix} y_i \\ y_{i+1} \\ y_{i+2} \\ y_{i+3} \end{bmatrix} = \begin{bmatrix} x_i & x_{i+1} & x_{i-2} & x_{i-3} \\ x_{i+1} & x_i & x_{i-1} & x_{i-2} \\ x_{i+2} & x_{i+1} & x_i & x_{i-1} \\ x_{i+3} & x_{i+2} & x_{i+1} & x_{i-} \end{bmatrix} \times \begin{bmatrix} c0 \\ c1 \\ c2 \\ c3 \end{bmatrix} + \ldots + \begin{bmatrix} x_{i-12} & x_{i-13} & x_{i-14} & x_{i-15} \\ x_{i-11} & x_{i-12} & x_{i-13} & x_{i-14} \\ x_{i-10} & x_{i-11} & x_{i-12} & x_{i-13} \\ x_{i-9} & x_{i-10} & x_{i-11} & x_{i-12} \end{bmatrix} \times \begin{bmatrix} c12 \\ c13 \\ c14 \\ c15 \end{bmatrix}$$

1024-point, radix-2 FFT (35.4 cycles)




A single DIF butterfly

$$\begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ a & -b & -a & b \\ b & a & -b & -a \end{bmatrix} \times \begin{bmatrix} In1\_r \\ In1\_i \\ In2\_r \\ In2\_i \end{bmatrix} = \begin{bmatrix} Out1\_r \\ Out1\_i \\ Out2\_r \\ Out2\_i \end{bmatrix}$$

**Versatility of the floating point co-processor**

### *MULTIPLICATION*

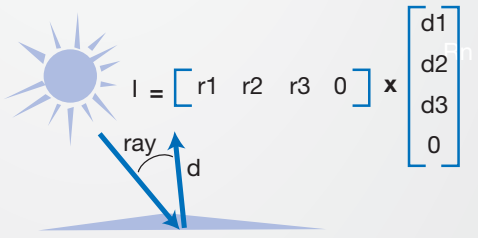
**Multiplication 3-D graphics geometry**

$$\begin{bmatrix} Y1 \\ Y2 \\ Y3 \\ 1 \end{bmatrix} = \begin{bmatrix} c11 & c12 & c13 & c14 \\ c21 & c22 & c23 & c24 \\ c31 & c32 & c33 & c34 \\ c41 & c42 & c43 & c44 \end{bmatrix} \times \begin{bmatrix} x1 \\ x2 \\ x3 \\ 1 \end{bmatrix}$$

A single SuperH instruction, FTRV, can perform this matrix-vector multiplication every 4 cycles.

### *INNER PRODUCT*

**Surface judgement brightness calculation source**



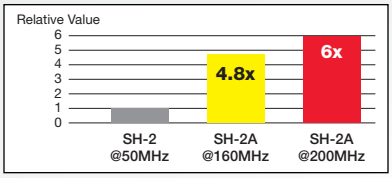

A single SuperH instruction, FIPR, can perform this inner-product multiplication every cycle.

**Powerful 4-way FPU for 3-D graphics**

## SH-2A Enhancements

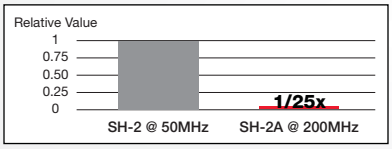
**Higher Execution Performance**

- Superscalar gives 1.5x more performance at the same MHz
- SH-2A = 6x the performance of SH-2



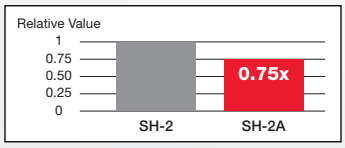

**Faster Interrupt Response Time**

- **SH-2:** 37 cycles; **SH-2A:** 6 cycles
- SH-2A = 1/25 the response time of SH-2




**Denser Program Code Size**

- Improved C compiler and additions to instruction set provide 25% code size reduction

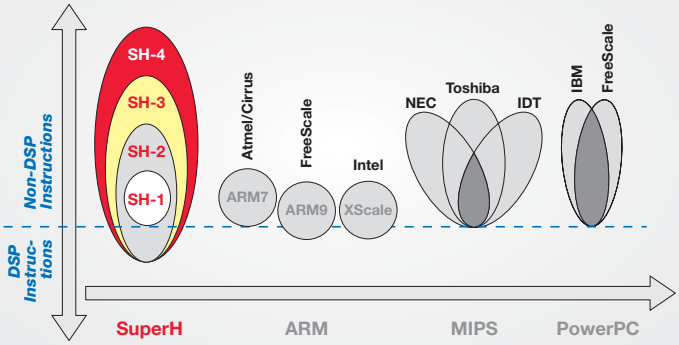



## SH-4A Enhancements

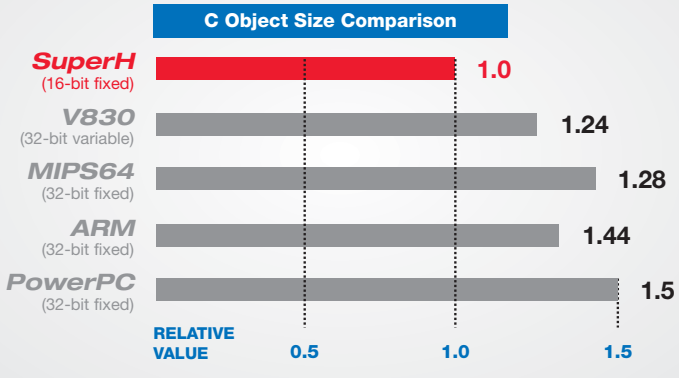
| | SH-4A | SH-4 |
|---|---|---|
| **Higher Performance at Lower Power** | 600 MHz @ 1.25V | 240 MHz @ 1.5V |
| **Improved Micro-Architecture** | Superscalar 7-Stage Pipeline | Superscalar 5-Stage Pipeline |
| **Improved FPU Architecture** | 10-Stage Pipeline | 5-Stage Pipeline |
| **Larger Cache Size** | 32/32 KB I/O Cache 4-Way Set-Associative | 16/32 KB I/O Cache 2-Way Set-Associative |
| **Greater Bandwidth Bus Architecture** | SuperHyway 3 Independent Buses | Shared Bus |
| **Instruction Set Architecture** | 103 Instructions | 91 Instructions |

## *TOP REASONS TO SELECT SuperH*

### Upward Code Compatibility




### SuperH Code Efficiency




### Total upward code compatibility

The roadmap for the SuperH processor product line is upwardly code compatible. This compatibility enables a faster time-to-market with further amortization of prior engineering investment and preservation of previously written software.

- Processor choice from 10 to 1080 MIPS
- Large selection of devices within each family

### Best code efficiency

- 16-bit instruction length for high code density
- Up to 40% less memory footprint than 32-bit instructions
- Up to 40% more data in cache than 32-bit instructions
- Twice the number of instructions loaded on the SDRAM bus

## *TOP REASONS TO SELECT SuperH*

### Balanced power/performance

**The fast speeds that SuperH devices provide would not be usable by portable applications if the chips' power dissipation was excessive. Therefore, Renesas has designed the RISC and RISC/DSP devices in low-power sub-micron CMOS processes with low-voltage capabilities. Low static operating current is achieved in all circuit designs; low dynamic (peak) currents are guaranteed by logic and circuit design.**

- Power-reducing techniques used in cache design
  - The sense amplifiers utilize SRAM circuit-design techniques that reduce word-line voltage swings; this permits lower currents to be used without sacrificing speed
  - A unique cache-way-enable circuit minimizes power demands by turning on the sense amplifiers only in that portion of the cache that has a "hit" in a given access; this reduces the cache data array's operating current by 75%
- Software-controlled power-reduction mechanisms:
  - Each device family offers a selection of power-reduction techniques from a palette that includes Standby and Sleep modes, clock-speed control and selective module shutdown
  - Low operating and standby currents for longer battery life.
- Hardware acceleration further reduces power consumption
  - Video, imaging, graphics, and security engines significantly improve computational speeds while minimizing power consumption

### High integration

**Renesas meets the dual needs for compact devices and low system cost by providing a broad choice of on-chip memories and peripherals in the SuperH series.**

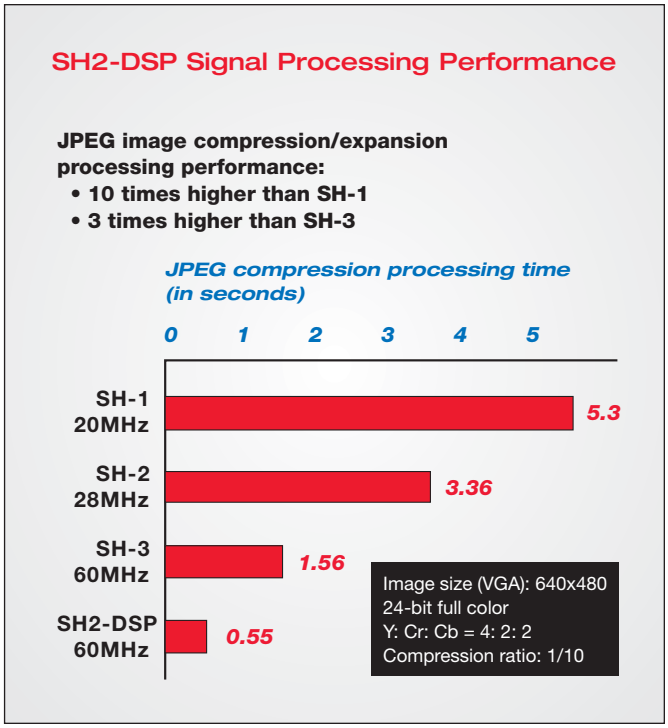
- Large size and high performance on-chip memory: Up to 1MB on-chip flash memory, up to 128KB on-chip RAM, and up to 32KB instruction and 32KB data cache
- 4- to 12-channel DMAC, 2 to 5 SCIs, 16-bit and 32-bit timers (3 to 34 channels), up to 149 I/O ports, RTC, analog interfaces (4 to 32 channels), $I^2C$, CAN (up to 2 channels), others
- All SuperH-series processors feature direct interfaces to external memories. The on-chip Bus State Controller, via the external bus, provides the specialized inputs, outputs and functions for different types, widths, and speeds of external memory (8/16/32-bit interfaces to DRAM, SDRAM, DDR-SDRAM, flash, ROM, etc.)

### Best cost/performance

**The SuperH architecture has a superior performance-to-price ratio (Dhrystone MIPS/$). The architecture's 16-bit RISC instruction set reduces system memory requirements, which lowers the overall cost of embedded system designs.**

### Superior floating point and DSP support

- The SuperH Family of processors with Floating Point Unit (SH-2A, SH-4, SH-4A) and DSP (SH2-DSP, SH3-DSP, SH-Mobile) support allow users to achieve more with less, reducing overall system cost and power consumption
- The SH-4 FPU is ideal for computer graphics and can be utilized to efficiently implement multimedia and networking operations



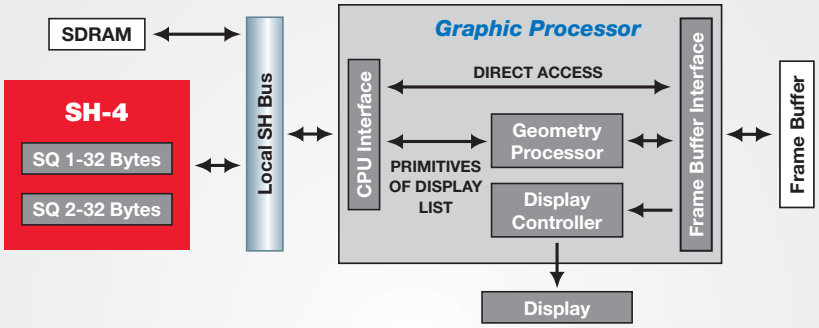
## TOP REASONS TO SELECT SuperH

### SuperH has 2D and 3D graphics capabilities

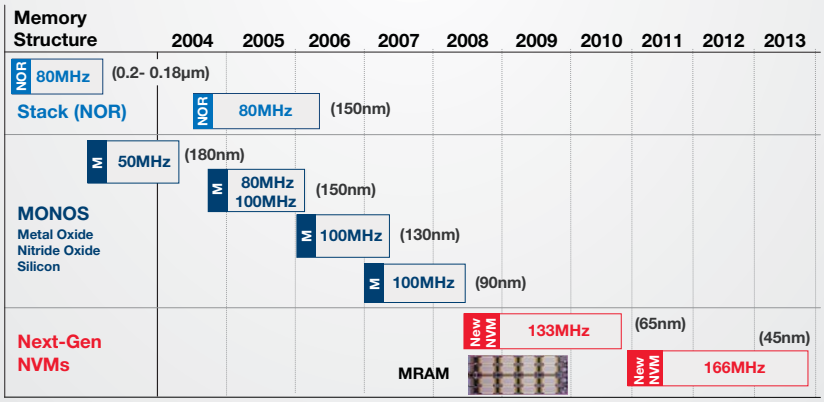
SuperH RISC and RISC/FPU microprocessors have excellent graphics-handling capabilities, allowing consumer-level products with highly integrated, enhanced features at popular prices. Systems built with other processor architectures require a separate graphics chip, which would increase complexity and add cost.

- **Superscalar architecture (SH-2A, SH-4, and SH-4A) –** Allows FPU operations to occur independently from non-FPU operations of the system. This optimizes the performance of the graphics calculations and minimizes flicker and graphic stalling.
- **Pair single-precision data transfer –** Data transfer can be performed by pair single-precision data transfer instructions, which enable two single-precision (each 32-bit) data items to be transferred for double the transfer performance.
- **Vector/matrix calculation –** Data can be processed efficiently because four multiplication operations and one addition operation are performed in parallel.
- **Geometric-operation instructions –** To enable high-speed computation with a minimum of hardware, geometric-operation instructions perform approximate-value computations.
- **The SH-4 supports two 32-byte store queues** (SQ) to perform high-speed burst writes to external memory. While the contents of one SQ are being transferred to external memory, the other SQ can be written to without a penalty cycle. This functionality is especially useful to transfer video, graphic or display list data to the frame buffer of the graphic processor.

**Fast Data Transfers to Frame Buffers Using the SH-4 Store Queues**




**SuperH Flash Roadmap**




### SuperH MCU flash technology leadership

Fourth-generation embedded flash, introduced in 2002, features single-cycle access to on-chip flash memory.

- 0.18µm process, flash size as high as 1MB
- Access as fast as 12.5ns @ 80MHz
- Up to -40°C to +125°C range
- Minimum endurance up to 10,000 erase/write cycles

## TOP REASONS TO SELECT SuperH

### SuperH standard, off-the-shelf solutions

Renesas' qualified middleware and proven reference boards comprise a complete set of solutions that can reduce overall chip count and minimize system cost, without sacrificing performance. These solutions allow a faster time to market.

### SuperH offers broad OS support

- SuperH offers a broad range of operating system choices to accommodate diverse applications.

### Sophisticated on-chip debug controller

- Hardware Break Controller provides 2 to 4 independent hardware breakpoints
- Advanced User Debug (AUD) on SH-3 and SH-4 devices provides trace capability
- Third parties offer tools that support the SuperH on-chip debug by utilizing the SuperH hardware resources in the RTOS debug environment
- JTAG BSDL is available for SH-3, SH3-DSP, SH-4, and SH-4A

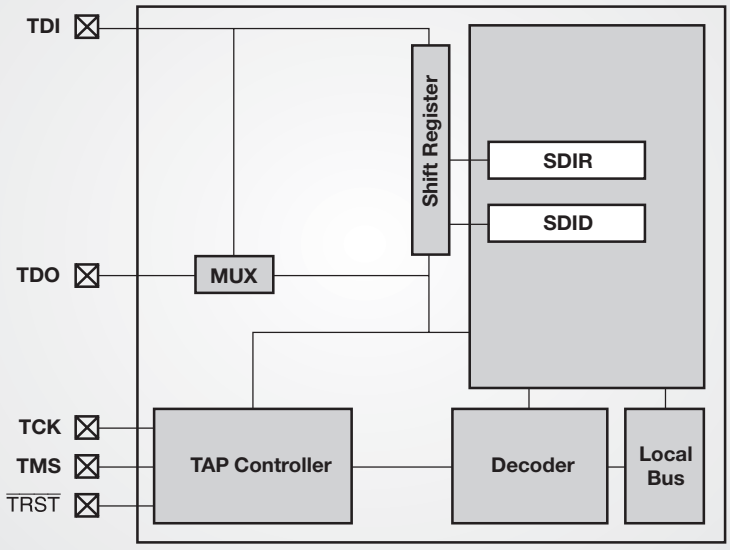
  [JTAG = Joint Test Action Group, a standard developed for boundary scan test. BSDL = boundary scan debug layer]
- Emulators are available from Renesas and third-party suppliers
- Development environments are available from Renesas and third-party vendors

### User Debugging Interface (UDI)

- Supplied with E10A-USB and E200F in-circuit emulators (see page 20)
- The main unit of the emulator is connected through the UDI port to the user's system

SuperH Multimedia Solution Example

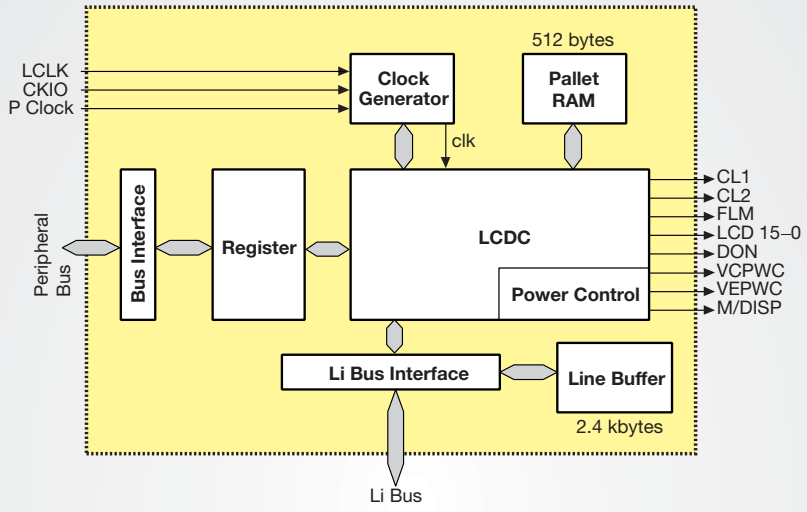
User Debugging Interface (UDI)



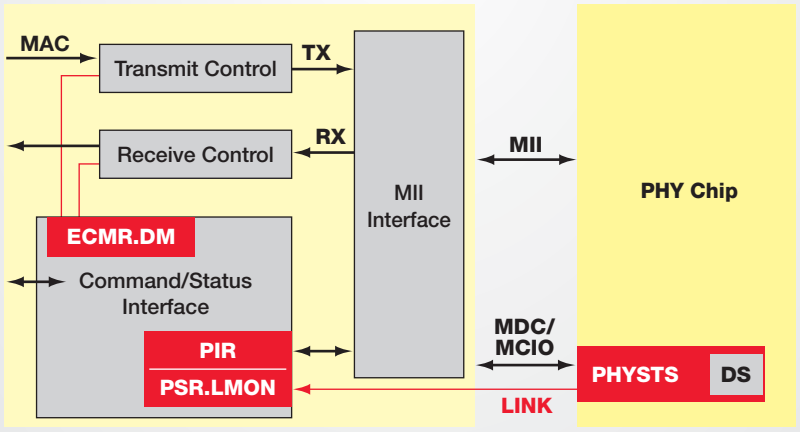
## LCD Controller

- From 16x1 to 800x600 pixels (SVGA) can be supported
- 11/2/4/6/8/16/18/24 bpp (bit per pixel) with 24-bit color pallet
- 1/2/4 bpp grayscale
- 8-bit frame rate controller
- Supports data formats for STN/dual-STN/TFT panels (8/12/16/18/24-bit bus width)
- Supports variations of the burst length in reading from the synchronous DRAM to achieve high data-read speeds
- Supports inversion of the output signal, if necessary, to match the LCD panel's signal polarity
- Hardware-rotation mode is included to support the use of landscape-format LCD panels as portrait-format LCD panels
- Power control function
- A unified memory architecture is adopted for the LCD controller so the image data for display is stored in system memory

### LCD Controller Block Diagram




### EtherC Function Block Diagram




## Ethernet MAC

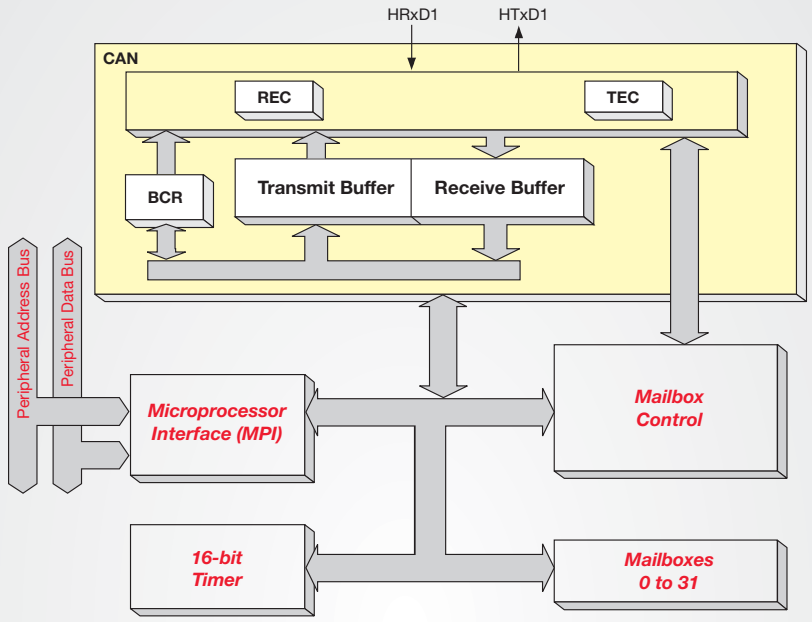
- MAC (Media Access Control) functions
  - Data frame assembly/disassembly (IEEE802.3-compliant frame)
  - CSMA/CD link management (collision avoidance, processing in case of collision)
  - CRC/PAD processing
  - Built-in FIFO (2KB for Tx, up to 8KB for Rx)
  - Supports full-duplex and half-duplex transmission/reception
  - Short packets/long packets
- Compatible with MII (Media Independent Interface), RMII (Reduced MII), and GMII (Gigabit MII) standards
  - Converts 8-bit data stream from MAC layer to MII nibble data stream (4 bits)
  - Station management (STA) functions
  - 18 TTL-level signals (5V or 3.3V interface)
  - Variable transfer rate: 10/100/1000Mbps (based on PHY chip features)
- Magic Packet™ (with wake-on-LAN output)
- CAM (Contents Addressable Memory) Interface

Peripherals

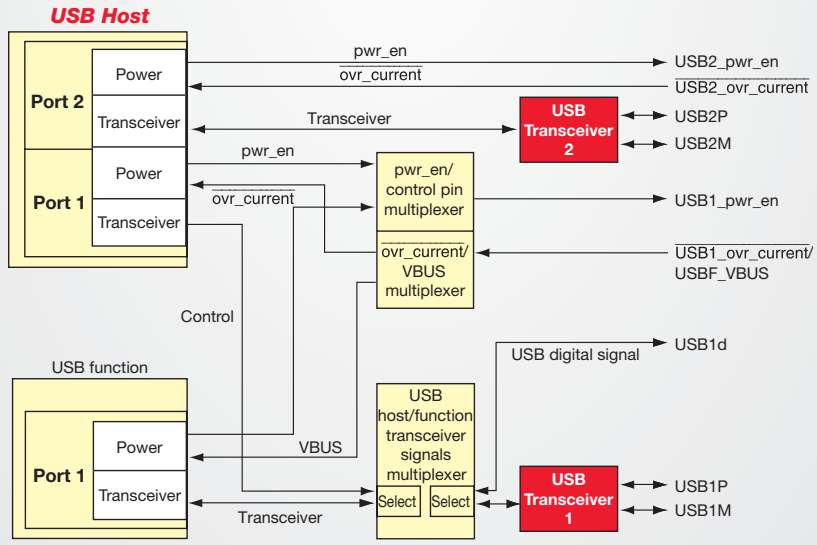
## Controller Area Network (CAN)

- CAN version: Bosch 2.0B active compatible
  - Communication systems: NRZ (Non-Return to Zero) system (with bit-stuffing function)
  - Broadcast communication system
  - Transmission path: Bi-directional 2-wire serial communication
  - Communication speed: Max. 1Mbps (at 40MHz operation)
  - Data length: 0 to 8 bytes
- Number of channels: 1 or 2
- Data buffers: 32 (one receive-only buffer and 31 buffers which can be set for transmission/reception)
- Data transmission: Two methods
  - Mailbox (buffer) number order (high-to-low)
  - Message priority (identifier) reverse-order (high-to-low)
- Supports 12 CPU interrupts
- Supports 7 operating modes
- 16-bit free-running timer (FRT) with flexible clock sources and prescaler
- Other features
  - DTC can be activated by message reception mailbox

### CAN Block Diagram




### USB Block Diagram




## Universal Serial Bus

- Compatible with Universal Serial Bus standard ver. 2.0
- Four transfer modes (Control, Interrupt, Bulk, Isochronous)
- Root Hub function
- Offers a range of modes: high-speed mode (480Mbps), full-speed mode (12Mbps) and low-speed mode (1.5Mbps)
- Overcurrent detection feature
- Up to 127 end points control (Host) and 4 end points (Function) can be specified
- On-chip transceiver (multiplex Host or Function)

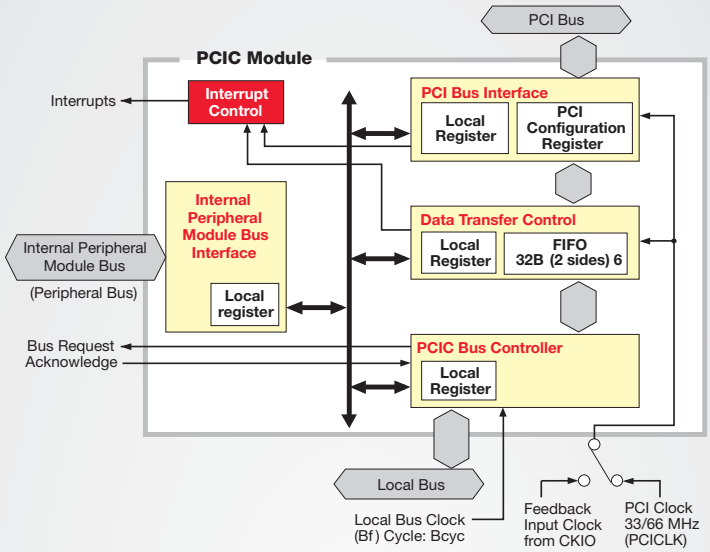
## Peripheral Control Interconnect (PCI)

- Compatible with PCI bus operating speeds of 33MHz/66MHz
- Compatible with 32-bit PCI bus
- Up to four PCI master devices running at 33MHz, or one PCI master device at 66MHz, can be connected
- Arbitration control is available as a PCI host function
- Can operate as master or target
- When operating as master, PIO and DMA transfer are available
- Four DMA transfer channels
- Six 32-bit x 16 longword internal FIFO (one for target reading, one for target writing, and four for DMA transfer)
- SRAM, DRAM, SDRAM, DDR-SDRAM, and MPX can be used as external memory for PCI bus data transfers
- 32-bit or 16-bit memory data bus for data transfers with PCI bus (32-bit bus when connected to SDRAM or DDR-SDRAM)
- Support for big-endian and little-endian local bus (PCI bus operates with little endian, while internal bus for peripheral modules operates with big endian)

## DMA Controller (DMAC)

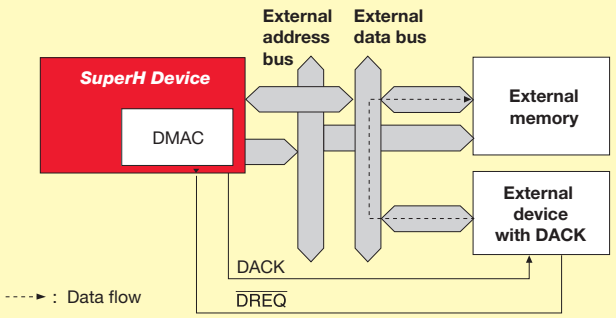
- Up to twelve channels
- Choice of 8-bit, 16-bit, 32-bit, 64-bit, or 32-byte transfer data length
- Choice of address mode; single or dual; choice of bus mode: cycle steal mode or burst mode
- Two types of DMAC channel priority ranking: fixed-priority mode and round-robin mode

### PCI Block Diagram



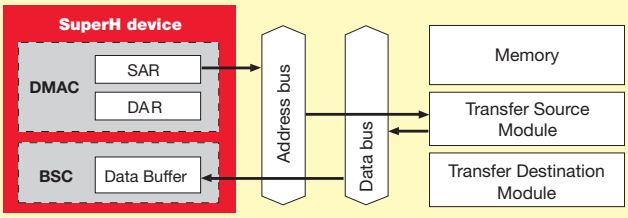

### DMAC: Single and Dual Address Modes

***SINGLE-ADDRESS MODE: Parallel read and write***

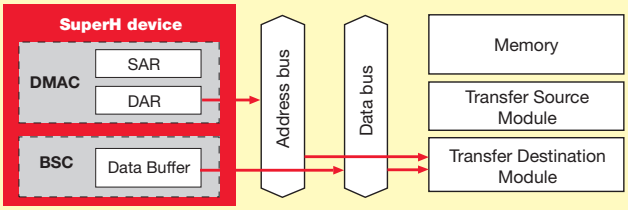



***DUAL-ADDRESS MODE: Two-cycle read and write***

**1st bus cycle:** Taking the SAR value as the address, data is read from the transfer source module and stored temporarily in the data buffer in the Bus State Controller (BSC).




**2nd bus cycle:** Taking the DAR value as the address, the data stored in the BSC's data buffer is written to the transfer destination module.



- An interrupt request can be sent to the CPU on completion of the specified number of transfers
- Various DMAC transfer requests are provided:
  - External request
  - On-chip peripheral modules (Transfer requests from the SCI, SCF, and TMU can be accepted on all channels.)
  - Auto-request (A transfer request is generated automatically within the DMAC)
- Channel functions: different transfer modes can be set for each channel

## Data Transfer Controller (DTC)

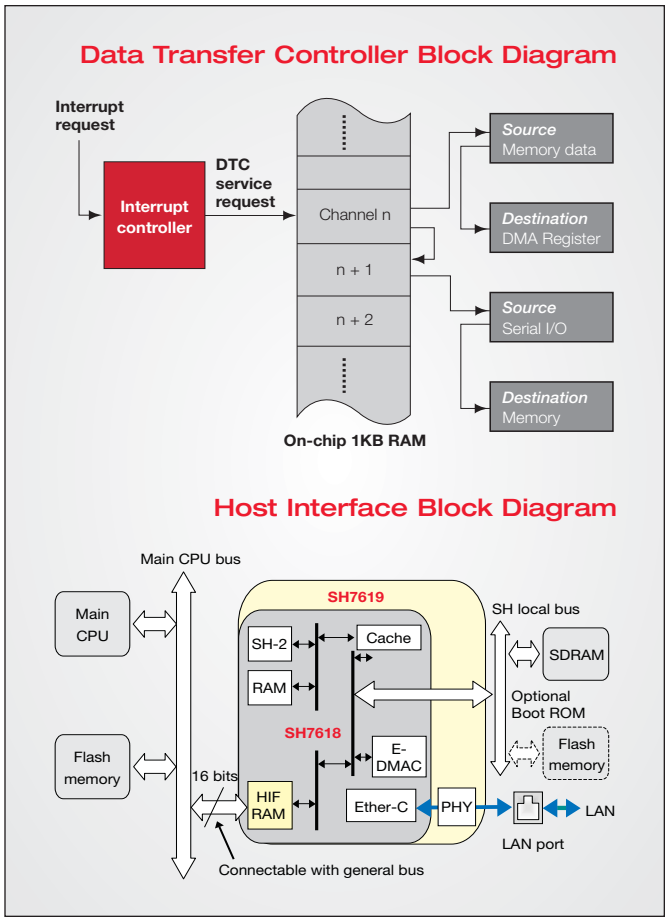
- Transfer possible over any number of channels
- 3 transfer modes: normal, repeat, and block transfer
- One activation source can trigger a number of data transfers (chain transfer)
- Direct specification of 32-bit address space
- Activation by software allowed
- Transfer can be set in byte, word, or longword units

## Host Interface (HIF)

- Connectable to the main CPU with parallel bus
- HIF boot function eliminates the need for boot ROM

## Motor Management Timer (MMT)

- Triangular-wave comparison-type 6-phase PWM waveform output with non-overlap dead times
- Non-overlap times generated by timer's dead time counters decrease torque pulsations/harmonics for improved voltage utilization
- Toggle output synchronized with PWM period
- PWM output halted by external signal
- PWM duty programmable between 0 and 100%
- Output-off functions
- Adjustable carrier frequency for low switching losses and less audible noise




## Multi-function Timer Unit (MTU)

- Up to 12-phase PWM output with synchronous operation
- 2-phase encoder pulse up/down count
- Counter cascade mode to 32-bit counter
- High sink current (15mA) for 6 pins; can directly drive opto-isolators
- A/D converter trigger signal can be generated
- Dead time can be generated automatically

## Analog Interfaces

- 4- to 32-channel 10-bit successive-approximation A/D converter
  - Precise current detection for current control
  - Three sample-and-holds with maximum conversion time of 5.4 microseconds
- 2 channel 8-bit D/A converter

Peripherals

## Overview

Renesas and the many third-party suppliers in the SuperH community provide a wide range of hardware and software tools and other support services. Renesas offers products that cover all stages of the development of embedded systems that use SuperH microcontrollers and microprocessors.

- **Evaluation**—Low-cost or no-cost Renesas tools make it easy to discover the capabilities of SuperH MCUs and test the problem-solving power of the tools themselves, including the High-performance Embedded Workshop (HEW) software development and debugging environment. A free downloadable evaluation version lets you evaluate the ability of the Renesas C/C++ compiler to generate efficient code, and evaluation boards enable you to immediately test that code on known working hardware. In addition, the Renesas Interactive remote engineering laboratory gives you the ability to use your own PC to obtain hands-on experience with powerful software and hardware tools before purchase.
- **Debugging**—When you begin working on the design of your system, you can develop code using the full unlimited compiler in exactly the same HEW environment. To track down bugs, use Renesas' on-chip and full in-circuit emulators, which have powerful specialized debugging hardware for trapping specific conditions and recording program activity.
- **Final Programming**—Use Renesas' Flash Development Toolkit, which has an easy-to-use interface, to program your debugged application into any of the many SuperH MCUs that incorporate Renesas' mature on-chip flash memory technology.

All the tools required for developing SuperH-based applications are available from Renesas distributors. These tools have been developed by groups within the worldwide Renesas organization, experienced engineers who have access to the designers of the devices themselves. Their insight and expertise ensure the best possible tool performance and support.

## Software

### Renesas' Integrated Development Environment

The High-performance Embedded Workshop (or HEW) is a graphical development environment for C/C++ compiler toolchains with an industry-standard look and feel. Through the use of menus, toolbars, status bars, dockable windows and context-sensitive local menus, HEW integrates key capabilities that can help you create and manage your embedded microcontroller software projects. Its capabilities include:

- Project creation and editing
- Graphical configuration of compiler tools
- Project make
- Debugging
- Version control

HEW provides enhanced functionality and an integrated instruction simulator that allows you to debug application code even when hardware isn't available. Also, the C/C++ compiler toolchains bundled with HEW generate code that executes faster and/or takes less memory space on Renesas processors.

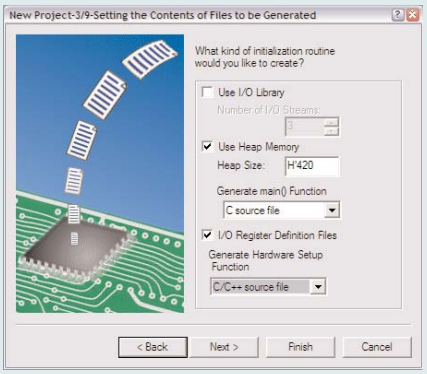
### *One familiar interface, many functions*

You can quickly learn the powerful tools you need for developing application code, and you have easy-to-use control over those tools.

Moreover, you can work with an interface that remains consistent across the entire range of Renesas MCUs and MPUs for greater efficiency. The interface is also highly customizable, so you can create an even more efficient environment for developing your application.

### *Wizards simplify start-up processes*

You can start projects fast by taking advantage of HEW's Project Generator "Wizards." Let them guide you through the selection of configuration options, debugger targets, and the creation of startup code.

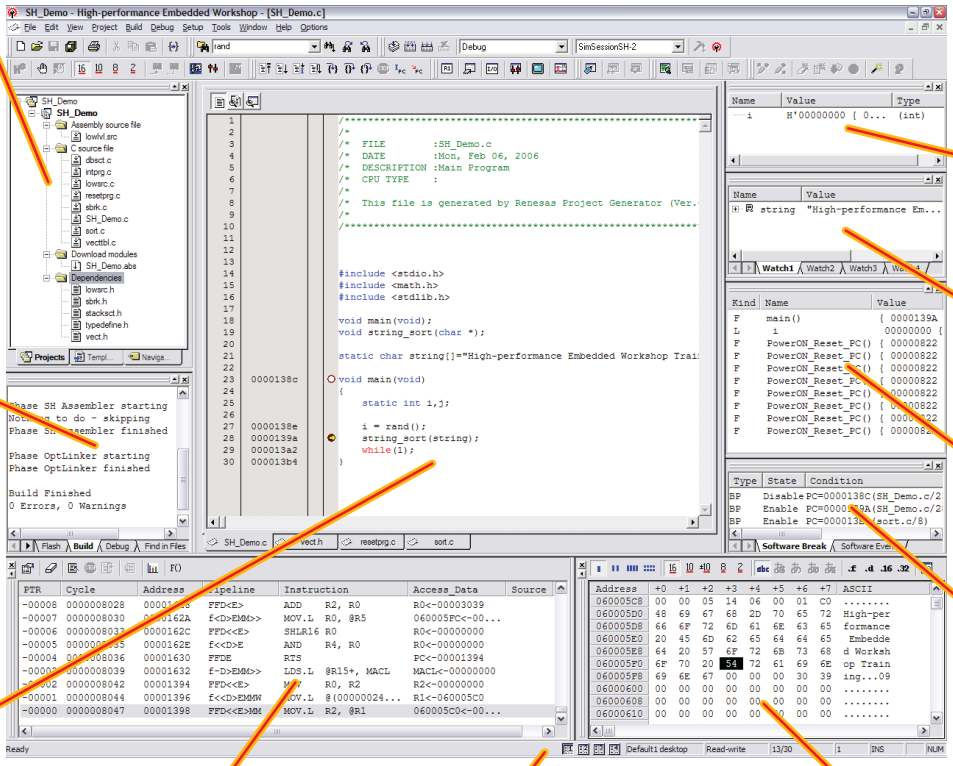


## HEW 4 Integrated Development Environment

**Project Manager**
– Graphical control of compiler/linker options
– Function browser
– Drag-and-drop code templates
– Built-in (or external) project make

**Output Window**
– Shows messages from build and find-in-files
– Linked to source in editor
– Version-control log

**Built-in Editor**
– Syntax sensitive coloring
– Multiple files open at once
– Source-level debugging




**Full Bus Trace**

**Virtual Desktop**
– Allows multiple screen layouts to be recalled at the click of a button

**Memory View**
– Highlights changed values

*New features to help optimize your application code*

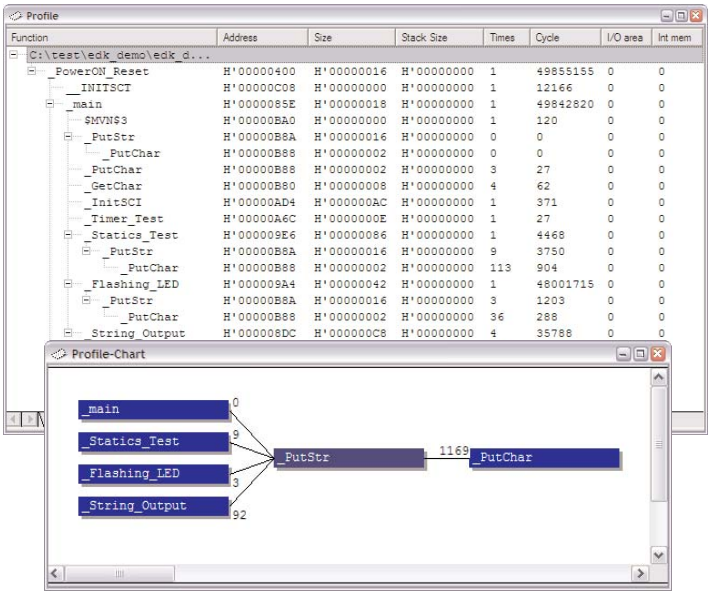
The integrated simulator/debugger has specific features and windows for testing the application code produced in the build process:

- Code profiling window (includes statistical and graphical displays)
- Performance analysis
- Code coverage window

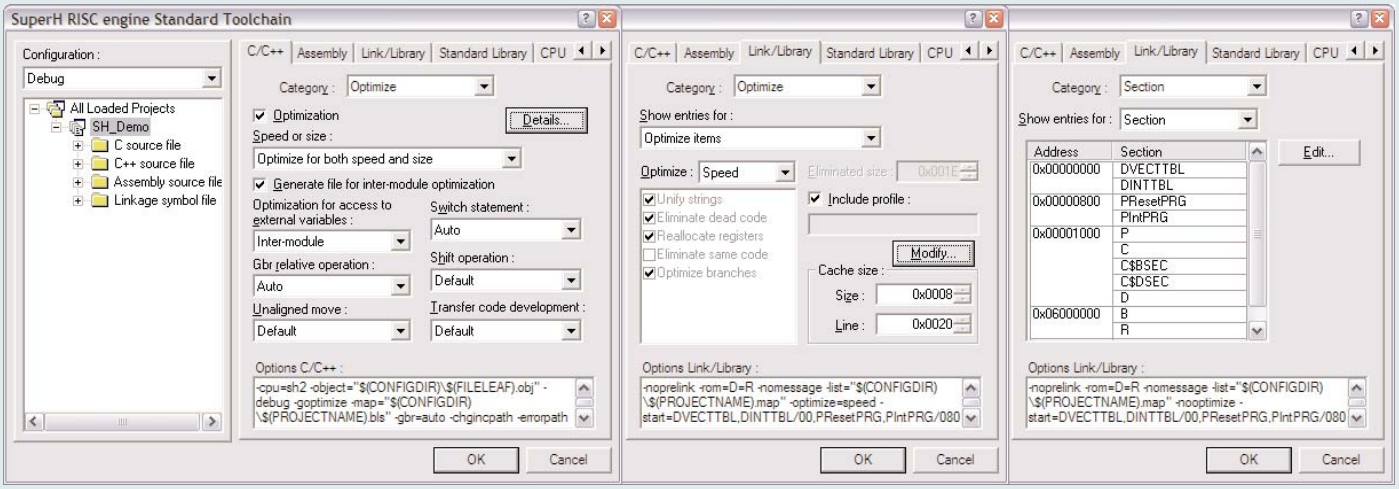
Additional analysis tools help you understand the operation and architecture of your embedded system application:

- Call Walker stack trace analyzer
- Link Map file viewer

## HEW Profile Tree and Chart views



## HEW Compiler Toolchain Options Dialogs




## ■ Software (continued)

### Optimized C/C++ code generation toolchains

The Renesas compiler toolchains (compiler, assembler and linker) support the full C++ language specification and are backward compatible with C. They have extensions for complete embedded system control directly from C, without requiring the use of any assembler code. These extensions cover:

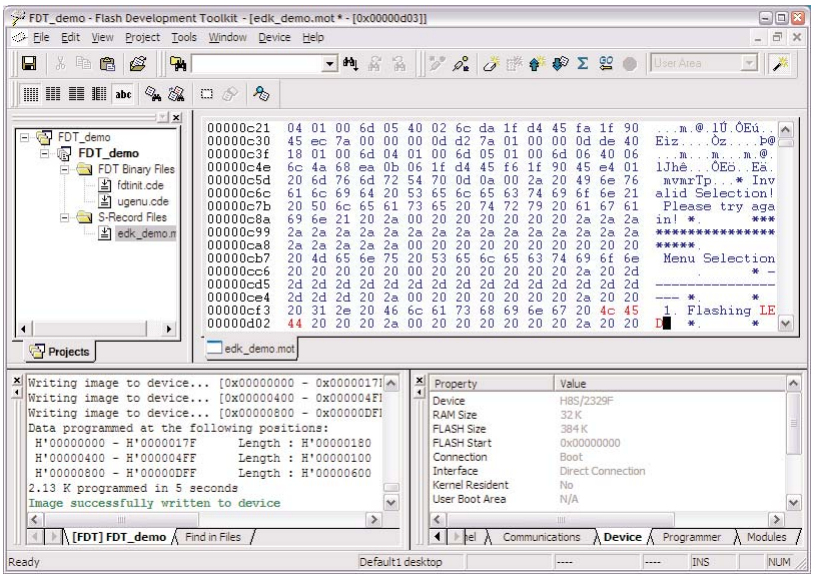
- Interrupt service routines
- Condition control register operations
- Sleep instruction
- Pseudo functions for instructions such as multiply-and-accumulate and decimal add and subtract
- Control of the optimized addressing and function call features of the device architecture and instruction set

The inter-module optimizing linker produces optimized software load modules by performing global optimizations on your application.

### Free evaluation HEW download

The flexible licensing technology in Renesas' compiler toolchains means you can download a free evaluation copy of HEW with the compiler and generate unlimited code for 60 days. This is very useful for benchmarking optimization efficiency and architecture performance. After 60 days, code size is limited to 256 Kbytes, which still allows you to evaluate the architecture or experiment with peripherals or, for smaller devices, even complete a full application, since the evaluation version is identical to the full version with the exception of the code size limits.

### Flash Development Toolkit



### HEW Integrated Debugging

Modular debug target support is provided directly within the HEW environment so you can build your application and debug without leaving HEW. A debug session wizard allows you to easily add a new debug target to your workspace:

- Instruction Simulator
- In-Circuit Emulators (E200F series)
- On-chip Emulators (E10A-USB, E8)
- Evaluation boards using a ROM-resident monitor

### Flash Development Toolkit

Renesas' Flash Development Toolkit (FDT) is an easy-to-use utility for programming your code into the on-chip flash memory of SuperH MCUs. You can create workspaces to combine several s-record files into one download image and save connection settings to easily manage device programming.

**FDT offers:**

- Direct USB connection for USB boot mode devices
- Serial communication at up to 115,200 baud
- Hex image editor
- Extensive messaging that helps hardware development

## Hardware

### Evaluation and Development Kits

Renesas' low-cost Evaluation and Development Kits (EDKs) are inexpensive ways to experience the performance of SuperH microcontrollers and microprocessors. Each kit comes complete with an EDK board and a CD-ROM that contains:

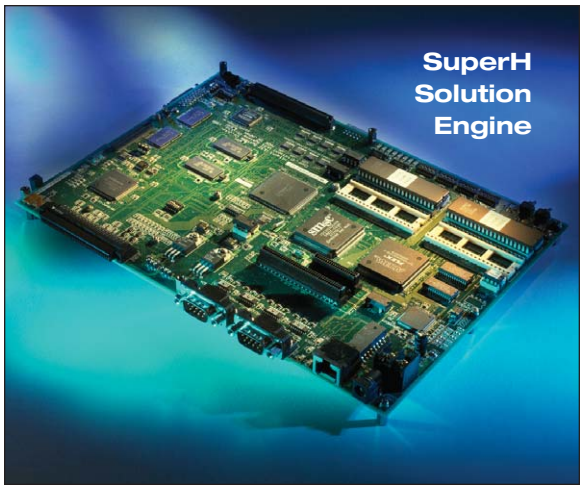
- Evaluation version of HEW with C/C++ compiler and a debug monitor
- Flash Development Toolkit (FDT)
- Quick-Start guide
- Full documentation with sample tutorials and a tutorial Project Generator plug-in for HEW

### Renesas Starter Kits

RSKs are the latest line of evaluation and development kits from Renesas. The target boards provide a standardized platform for all Renesas MCUs (H8, R8C, M16C, M23C and SuperH). The kit comprises all of the content of the EDK kits and – additionally – a USB on-chip debugger that provides full remote boot programming and debugging.


### SuperH Solution Engine

The SuperH architecture provides advantages in price, performance, power and code density. The Solution Engine family of development boards make implementing SuperH-based designs easy and provide complete system platforms ready for application development with spacious SDRAM and FLASH memory to enable development of large and complex programs. They also enable rapid evaluation of the SuperH architecture and available peripherals.




Multiple vendors support the Solution Engine platforms with real-time operating systems (RTOSs), board support packages and middleware to enable rapid product implementation for designs that require operating systems. The Solution Engine boards support

## Hardware (continued)

multiple SuperH devices. Typical features of the Solution Engine include:

- External flash for user code
- EPROM containing monitor code
- JTAG connector easily connects to E10A on-chip emulator
- Unbuffered CPU bus connectors provide direct connection to address data and control lines
- Expansion slot for daughter boards (buffered CPU bus provides direct connection to address data and control lines)
- I/O connectors (for SuperH peripheral signals)

### E10A-USB on-chip emulators

The E10A-USB emulators, designed to connect with Renesas' JTAG on-chip debugging interfaces, provide real-time debugging on the target device, using the dedicated debugging resources built into the target microcontroller in your user hardware. The on-chip emulators connect to the target system via an interface that can be used both to debug the system and to program the MCU's on-chip flash memory.

E10A-USB emulators use plug-and-play USB 2.0 compatible interfaces for easy connection to both notebook computers and desktop machines. These emulators offer:

- 255 PC breakpoints
- One hardware breakpoint on data and address
- The ability to save a record of up to the last eight branches
- On-chip flash programming

The E10A-USB emulator is available in two configurations:

- HS0005KCU01H (14pin H-UDI)
- HS0005KCU02H (14pin H-UDI + 36pin AUD)

Both provide on-chip debugging via the Renesas H-UDI (JTAG) interface.

### Advanced User Debug (AUD)

Renesas' Advanced User Debug interface allows you to trace real-time data out of the device while it is running in-system.


You can configure the AUD trace to stream source and destination branch addresses, memory accesses (from user-specified data buses and "windows" in the address space) and also source-level variables via a special software-trace function call.

This data is compressed on-chip, streamed out of the AUD port, and then captured in a dedicated trace buffer in the E10A-USB (HS0005KCU02H model only) or E200F (see next section).

### E200F Configurable On-Chip/In-Circuit Emulator

The E200F is an expandable emulation system for both on-chip and in-circuit debugging. It provides all of the same H-UDI (JTAG) and AUD debug features as the E10A-USB, but with enhanced capabilities and system expansion with add-on options.

#### *Enhanced Capabilities*

The E200F has a high-speed USB 2.0 host interface for fast debug file download and data upload. Eight AUD Event points allow you to halt on a match of AUD trace data such as branch source/destination address, windowed memory access and software data variable trace. Four external probe inputs and one external trigger output are also included.

#### *Performance Analysis*

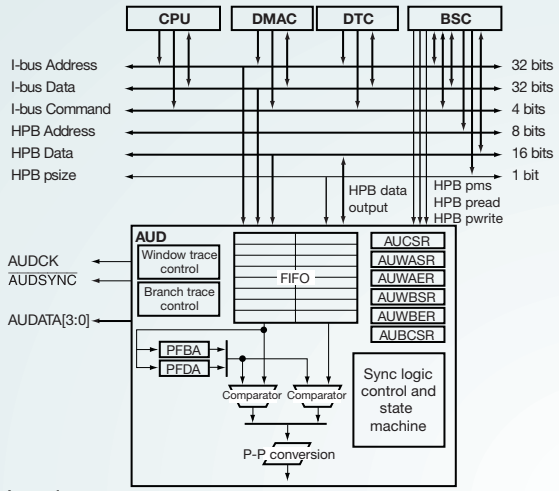
The E200F emulator provides three methods of application performance analysis:

- On-chip performance
- AUD performance analysis
- Real-time profiling

The real-time profiling method gives execution statistics for

## Advanced User Debug (AUD) Trace

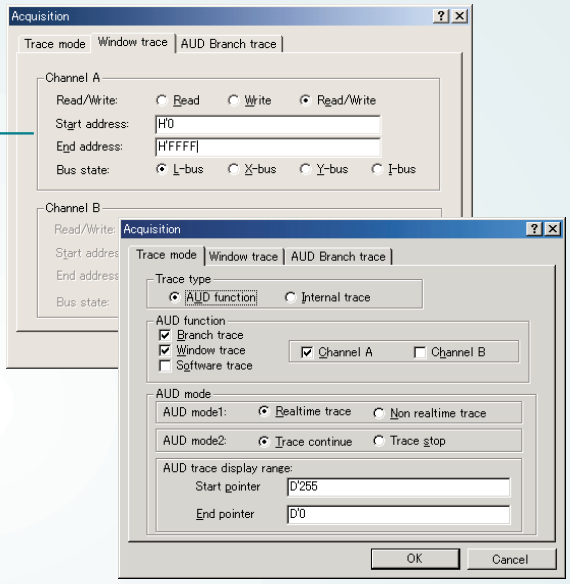
### AUD on-chip control logic



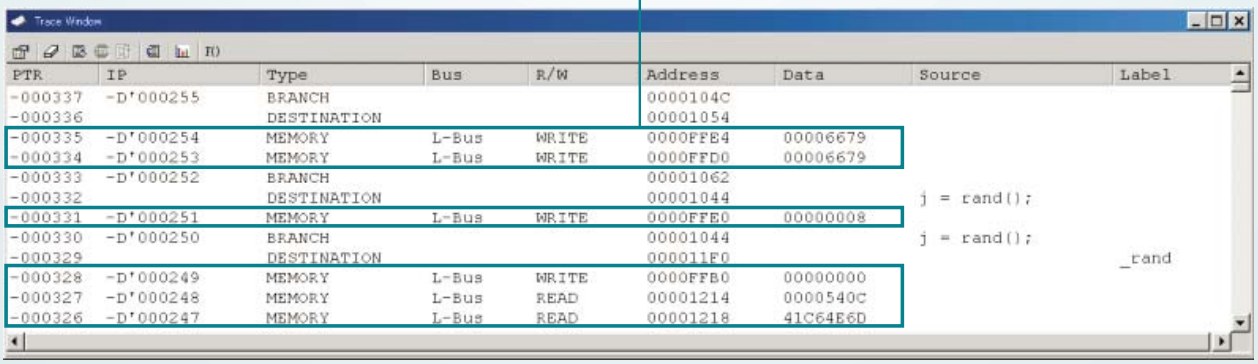

**Legend**

AUCSR : AUD control register
AUWASR : AUD window A start address register
AUWAER : AUD window A end address register
AUWBSR : AUD window B start address register
AUWBER : AUD window B end address register
AUBCSR : AUD bus master control register
PFBA : Previous full branch address
PFDA : Previous full data address

### AUD Configuration dialog in HEW




### AUD Trace View in HEW showing memory window trace




functions in up to 4MB of the system address space (8 x 512K blocks). An optional profiling expansion board increases the profiling capability to 12MB (24 x 512K blocks).

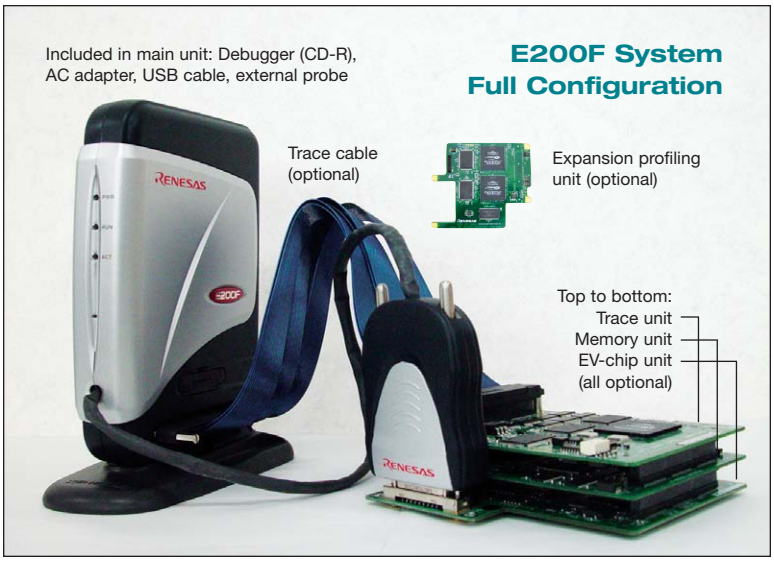
### *External Bus Trace*

You can further expand the E200F system by connecting the optional Bus Trace unit. This lets you synchronously trace 256K external bus cycles from the device in your target system and examine them in the HEW IDE.

The Bus Trace unit also provides 10 Bus Event points that you can use to control trace acquisition or halt program execution.

### E200F System Full Configuration

Included in main unit: Debugger (CD-R), AC adapter, USB cable, external probe



## ■ Hardware (continued)

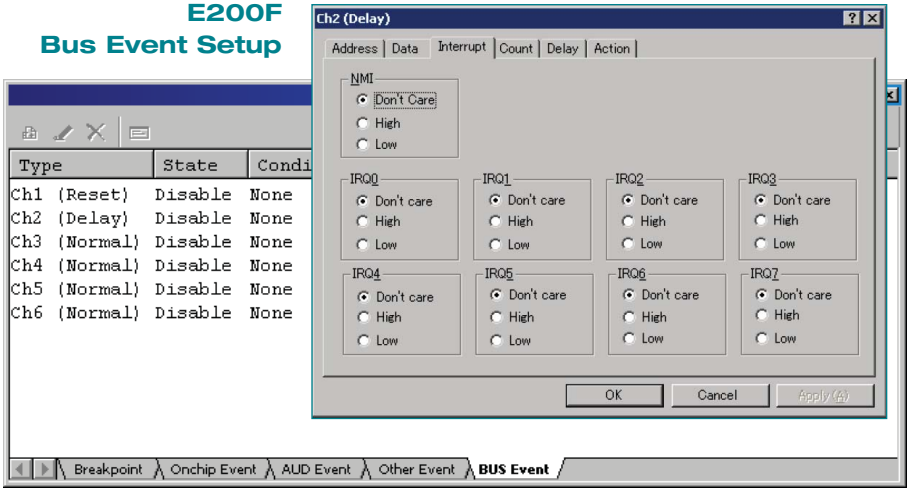
### *Evaluation Chip Unit*

The special "bond-out"chip on the optional Evaluation Chip unit brings out internal CPU buses, which – when used with the Bus Trace unit – give you full bus trace from within the device itself. The Evaluation Chip unit has connectors on the underside that can connect, via a user interface adaptor, to your target system in place of the regular chip. You can then emulate the device in your target system with access to all the E200F Emulator's enhanced debugging features – even with devices that lack the AUD trace output.

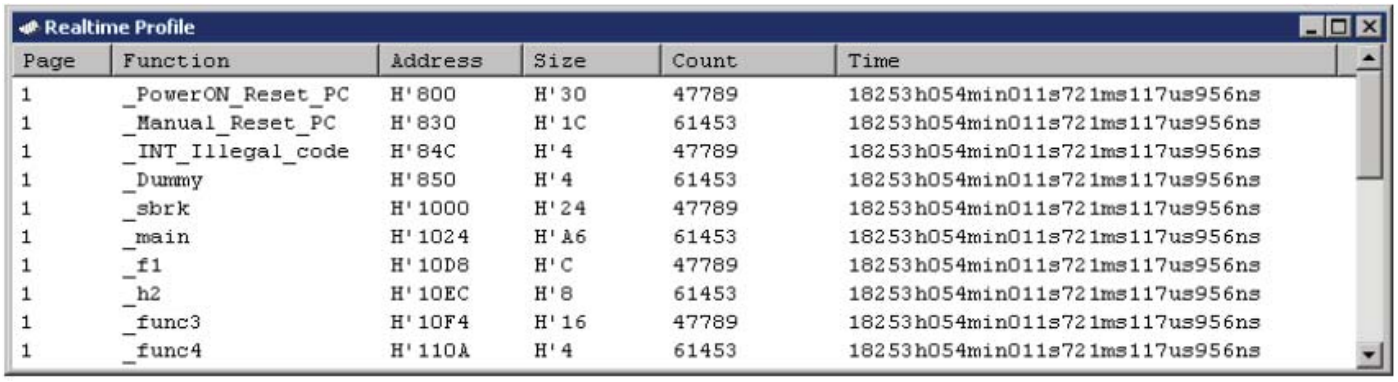
### *Emulation Memory Units*

The optional Emulation Memory units give you 8 or 16 Mbytes of system memory. When used with the Evaluation Chip unit, you can do real-time software debugging without any target hardware.

**E200F**
**Bus Event Setup**




## Real-time profiling




| Page | Function | Address | Size | Count | Time |
|---|---|---|---|---|---|
| 1 | _PowerON_Reset_PC | H'800 | H'30 | 47789 | 18253h054min011s721ms117us956ns |
| 1 | _Manual_Reset_PC | H'830 | H'1C | 61453 | 18253h054min011s721ms117us956ns |
| 1 | _INT_Illegal_code | H'84C | H'4 | 47789 | 18253h054min011s721ms117us956ns |
| 1 | _Dummy | H'850 | H'4 | 61453 | 18253h054min011s721ms117us956ns |
| 1 | _sbrk | H'1000 | H'24 | 47789 | 18253h054min011s721ms117us956ns |
| 1 | _main | H'1024 | H'A6 | 61453 | 18253h054min011s721ms117us956ns |
| 1 | _f1 | H'10D8 | H'C | 47789 | 18253h054min011s721ms117us956ns |
| 1 | _h2 | H'10EC | H'8 | 61453 | 18253h054min011s721ms117us956ns |
| 1 | _func3 | H'10F4 | H'16 | 47789 | 18253h054min011s721ms117us956ns |
| 1 | _func4 | H'110A | H'4 | 61453 | 18253h054min011s721ms117us956ns |

## SuperH Tool Selector

| Series | Group | Suggested Starter Kit or Reference Platform | E10A-USB On-chip Debug Emulator | E200F Full Emulator [2] | | | IDE [3] (C Compiler) |
|---|---|---|---|---|---|---|---|
| | | | | Base Unit | Evaluation chip board | User interface board | |
| SH-Tiny | 7125 | R0K571242S000BR | HS0005KCU01H | R0E0200F1EMU00 | R0E570800VKK00 | R0E571250CFK00 | RTA-HEWSH-1U |
| SH-2 | 7146 | EDK7145 | HS0005KCU01H | R0E0200F1EMU00 | R0E570800VKK00 | R0E571460CFJ00 | RTA-HEWSH-1U |
| SH-2 | 7086 | R0K570865S000BE | HS0005KCU02H [1] | R0E0200F1EMU00 | R0E570800VKK00 | R0E570860CFK00 | RTA-HEWSH-1U |
| SH-2A | 7211 | R0K572115S000BE | HS0005KCU02H [1] | R0E0200F1EMU00 | R0E572110VKK00 | R0E572110CFK00 | RTA-HEWSH-1U |
| SH-2A | 7201 | R0K572011S000BE | HS0005KCU02H [1] | - | - | - | RTA-HEWSH-1U |
| SH-2A | 7203 | R0K572030S000BE | HS0005KCU02H [1] | R0E0200F1EMU00 | - | - | RTA-HEWSH-1U |
| SH-2A | 7206 | MS7206SE01 | HS0005KCU02H [1] | R0E0200F1EMU00 | R0E572060VKK00 | R0E572060CFK00 | RTA-HEWSH-1U |
| SH-2 | 7618 | MS7618ACP01 | HS0005KCU01H | - | - | - | RTA-HEWSH-1U |
| SH-2 | 7619 | MS7619SE01 | HS0005KCU01H | - | - | - | RTA-HEWSH-1U |
| SH3-DSP | 7712 | MS7712SE01 | HS0005KCU02H [1] | - | - | - | RTA-HEWSH-1U |
| SH3-DSP | 7720 | MS7720RP02 | HS0005KCU02H [1] | - | - | - | RTA-HEWSH-1U |
| SH-4 | 7760 | MS7760CP02P | HS0005KCU02H [1] | R0E0200F0EMU00 | - | - | RTA-HEWSH-1U |
| SH-4A | 7780 | MS7780SE03 | HS0005KCU02H [1] | R0E0200F0EMU00 | - | - | RTA-HEWSH-1U |
| SH-4A | 7763 | MS7763SE02Y | HS0005KCU02H [1] | - | - | - | RTA-HEWSH-1U |

**NOTES:**
1. Includes AUD real-time trace support and both 36-pin AUD & 14-pin H-UDI target cables.
2. E200 emulation system, can operate with the base unit alone (see website for details).
3. Five-user pack and floating network licences also available (see website for details).

## Third-party Development Tools

Many third-party experts offer development tools supported by design services, RTOS, compilers, board-level solutions, custom firmware, and board-support packages (BSPs) to meet the needs of customers developing SuperH-based products. Product-ready single-board computers (SBCs) and application-specific reference designs offered by systems integrators are fully developed solutions designed for the lowest cost and highest performance. By embedding these engineered solutions in systems, customers can greatly reduce overall system design/debug time and development schedule risk because the board design, integration and debug, driver development, driver optimization, and driver and board testing have already been done. As a result, customers can bring end products to market months faster.

WIND RIVER

QNX RTOS

CMX COMPANY

Microsoft® Windows® Embedded Partner

Linux

Accelerated Technology® NUCLEUS

montavista

expresslogic

### Third-party RTOS Support

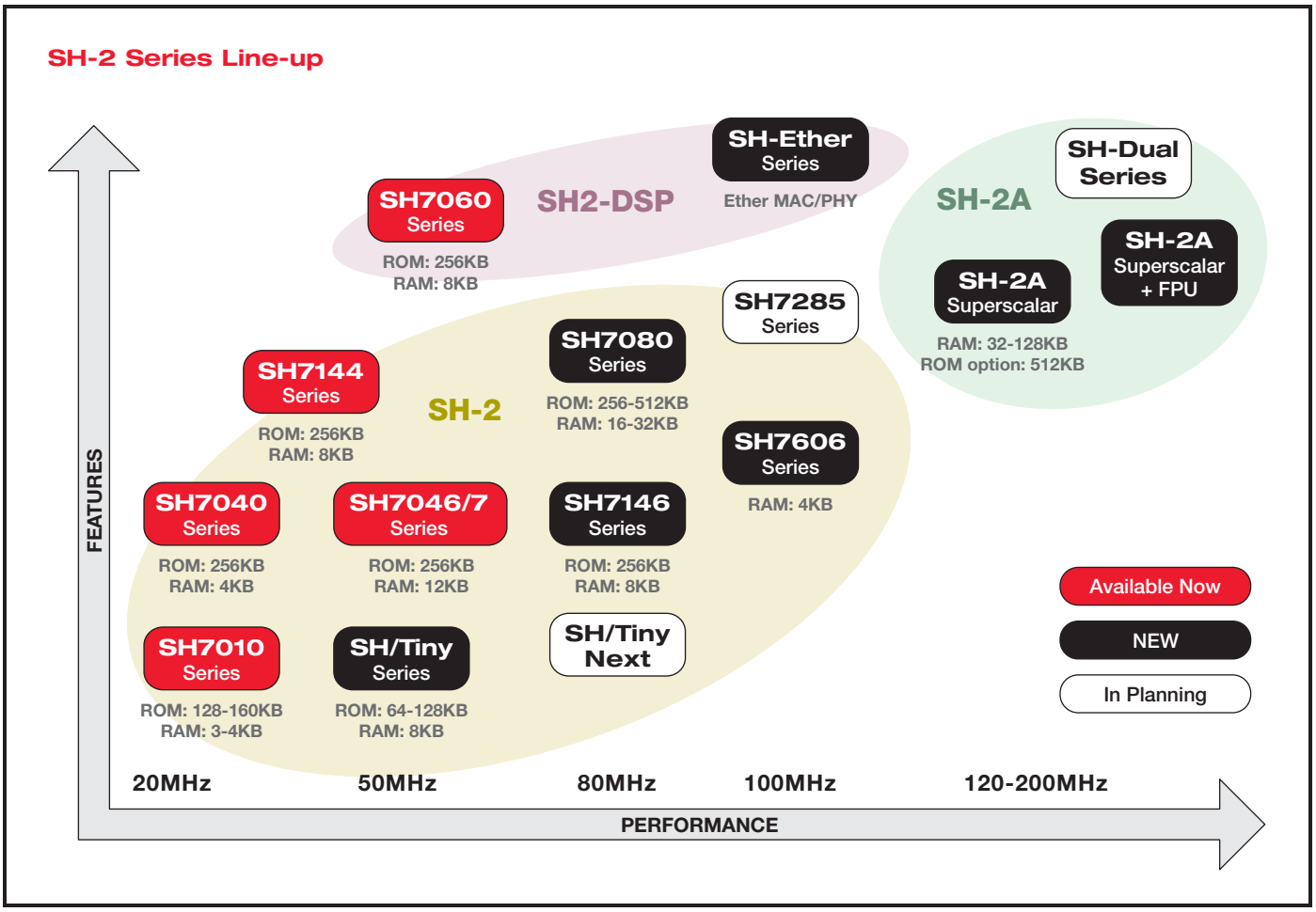
| | SH-1 / SH-2 | SH-2A | SH-3 | SH-4 | SH-4A | SH-Mobile |
|---|---|---|---|---|---|---|
| **ATI Nucleus** | ✓ | soon | ✓ | ✓ | ✓ | ✓ |
| **CMX** | ✓ | | ✓ | ✓ | ✓ | |
| **Express Logic ThreadX** | ✓ | soon | ✓ | ✓ | | |
| **LynxOS** | | | | ✓ | | |
| **Microsoft Windows®CE** | | | ✓ | ✓ | ✓ | |
| **Montavista Linux** | | | ✓ | ✓ | | |
| **Open Source Linux** | soon | | ✓ | ✓ | ✓ | ✓ |
| **ucLinux** | | soon | | | | |
| **OS9** | | | ✓ | ✓ | | |
| **QNX** | | | | ✓ | soon | |
| **WindRiver VxWorks** | ✓ | | ✓ | ✓ | soon | |

### Third-party Compiler Support

| | SH-1 / SH-2 | SH-2A | SH-3 | SH-4 | SH-4A | SH-Mobile |
|---|---|---|---|---|---|---|
| **Altium** | ✓ | | ✓ | ✓ | | |
| **GAIO** | ✓ | ✓ | ✓ | ✓ | | |
| **GHS** | ✓ | ✓ | ✓ | ✓ | ✓ | |
| **GNU** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| **IAR** | ✓ | | ✓ | ✓ | | |
| **Metrowerks** | ✓ | | ✓ | ✓ | | |

### Third-party System Integrators

| | Hardware | WindowsCE | Linux | Other | Website |
|---|---|---|---|---|---|
| **BSquare** | | ✓ | | | www.bsquare.com |
| **CalAmp** | ✓ | ✓ | ✓ | ✓ | www.calamp.com |
| **California Software Labs** | ✓ | ✓ | ✓ | | www.cswl.com |
| **JJPlus** | ✓ | | ✓ | | linux.jjplus.com |
| **Logic Products Development** | ✓ | ✓ | | | www.logicpd.com |
| **Software Research Associates** | | | ✓ | | www.sraoss.com |
| **Systemic Realtime Design** | ✓ | | ✓ | ✓ | www.sysrtime.com |
| **TrygTech** | | ✓ | | | www.trygtech.com |
| **Kenati Technologies** | | | ✓ | ✓ | www.kenati.com |
| **Trinity Convergence** | | | ✓ | | www.trinityconvergence.com |
| **TrollTech** | | | ✓ | ✓ | www.trolltech.com |




## Features

- Large size and high-performance on-chip memory: Up to 512KB on-chip flash memory and up to 32KB on-chip RAM
- Direct connection to external memory (e.g., SDRAM, SRAM and Flash) via 8/16/32-bit external data bus
- Devices with on-chip DSP enable accurate current/position control. The RISC/DSP devices allow concurrent monitoring and controlling of a system
- Special advanced Motor Management Timer with outputs for 6-phase PWM waveform (complementary/reset-synchronized) with programmable dead-time for 3-phase motor control
- Special Multi-function Timer Unit 3-phase motor controller includes 2 quadrature encoding channels for speed/position detection of rotor
- MTU and MMT have error input for emergency PWM shutdown
- Synchronized A/D converter enables precise current detection for motor control
- Industry-standard CAN interface for networking communication in applications such as factory automation
- Excellent MIPS/watt and low-power support, as well as low-voltage options
- On-chip debug hardware allows low-cost software debugging; no in-circuit emulator required
- Other on-chip peripherals include DMAC, DTC, SCI, up to 149 I/O ports, etc.

## Applications

**Industrial:** AC/DC drives, inverters, servos/motion controllers, robotics, machine tools, factory automation

**Consumer/Office Appliances:** Air conditioners, washers, refrigerators, DVD recorders, digital cameras, LCD projectors, multi-function printers, seismic monitoring systems, etc.

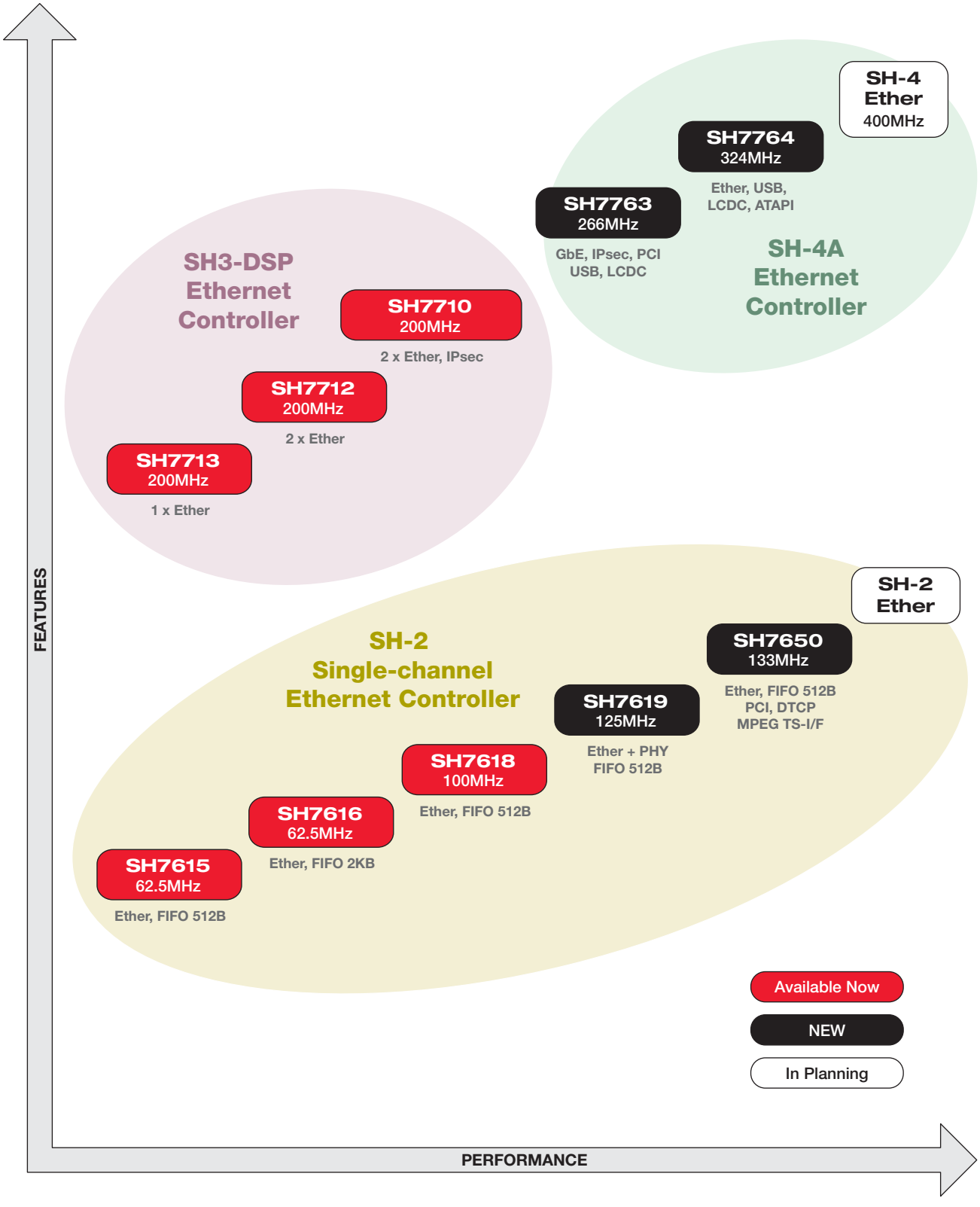
**Automotive:** Power door closers, seat positioners, starter/generators, air conditioners, electric power steering, etc.

**Medical:** Heart-rate monitors, dental equipment, etc.

## SH-2 Series Selector Guide

| Series | Group | Device Number | Flash (Kbytes) | RAM (Kbytes) | Vcc min | Vcc max | max MHz @ Vcc max | Power Down Modes | 8-bit timers | 16-bit timers | Watchdog Timers | Motor Control PWM Timer | A/D 10-bit resolution | D/A 8-bit resolution | Serial (sync/async) | DTC | DMA Channels | External Interrupts | GPIO | Special Features | Package Code |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SH-2 | 7046 | HD64F7046F50V | 256 | 12 | 4.0 | 5.5 | 50 | 3 | - | 5 | 1 | 1 | 12 | - | 2 | Y | - | 5 | 54 | MTU, CMT, MMT | FP-80Q |
| | 7047 | HD64F7047F50V | 256 | 12 | 4.5 | 5.5 | 50 | 4 | - | 5 | 1 | 1 | 16 | - | 3 | Y | - | 5 | 69 | MTU, MMT, CAN | P-100M |
| | 7144 | HD6417144F50V | - | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 82 | MTU, I²C, AUD | FP-112B |
| | 7144 | HD6417144FW50V | - | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 82 | MTU, I²C, AUD | FP-112B |
| | 7144 | HD64F7144F50V | 256 | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 82 | MTU, I²C, AUD | FP-112B |
| | 7144 | HD64F7144FW50V | 256 | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 82 | MTU, I²C, AUD | FP-112B |
| | 7145 | HD6417145F50V | - | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 106 | MTU, I²C, AUD | FP-144F |
| | 7145 | HD6417145FW50V | - | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 106 | MTU, I²C, AUD | FP-144F |
| | 7145 | HD64F7145F50V | 256 | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 106 | MTU, I²C, AUD | FP-144F |
| | 7145 | HD64F7145FW50V | 256 | 8 | 3.0 | 3.6 | 50 | 3 | - | 5 | 1 | 1 | 8 | - | 4 | Y | 4 | 9 | 106 | MTU, I²C, AUD | FP-144F |
| | 7146 | R5F71464AN80FPV | 256 | 8 | 4.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 12 | - | 3 | Y | - | 5 | 57 | MTU2, MTU2S, CMT | FP-80W |
| | 7146 | R5F71464AD80FPV | 256 | 8 | 4.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 12 | - | 3 | Y | - | 5 | 57 | MTU2, MTU2S, CMT | FP-80W |
| | 7146 | R5F71494AN80FPV | 256 | 8 | 4.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 12 | - | 3 | Y | - | 5 | 75 | MTU2, MTU2S, CMT | FP-100U |
| | 7146 | R5F71494AD80FPV | 256 | 8 | 4.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 12 | - | 3 | Y | - | 5 | 75 | MTU2, MTU2S, CMT | FP-100U |
| | 7080 | R5F70834AN80FTV | 256 | 16 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 73 | MTU2, MTU2S, CMT | TFP-100B |
| | 7080 | R5F70834AD80FTV | 256 | 16 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 73 | MTU2, MTU2S, CMT | TFP-100B |
| | 7080 | R5F70844AN80FPV | 256 | 16 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 84 | MTU2, MTU2S, I²C | FP-112E |
| | 7080 | R5F70844AD80FPV | 256 | 16 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 84 | MTU2, MTU2S, I²C | FP-112E |
| | 7080 | R5F70854AN80FPV | 256 | 16 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 108 | MTU2, MTU2S, I²C | FP-144L |
| | 7080 | R5F70854AD80FPV | 256 | 16 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 108 | MTU2, MTU2S, I²C | FP-144L |
| | 7080 | R5F70855AN80FPV | 512 | 32 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 108 | MTU2, MTU2S, I²C | FP-144L |
| | 7080 | R5F70855AD80FPV | 512 | 32 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 8 | - | 4 | Y | 4 | 9 | 108 | MTU2, MTU2S, I²C | FP-144L |
| | 7080 | R5F70865AN80FPV | 512 | 32 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 16 | - | 4 | Y | 4 | 9 | 134 | MTU2, MTU2S, I²C | FP-176E |
| | 7080 | R5F70865AD80FPV | 512 | 32 | 3.0 | 5.5 | 80 | 4 | - | 11 | 1 | - | 16 | - | 4 | Y | 4 | 9 | 134 | MTU2, MTU2S, I²C | FP-176E |
| | 7606 | HD6417606BG100V | - | 4 | 3.0 | 3.6 | 100 | 3 | - | - | 1 | - | - | - | 3 | - | - | 9 | 78 | HIF, CMT, SDRAM, PCMCIA | BP-176V |
| | 7606 | HD6417606BGN100V | - | 4 | 3.0 | 3.6 | 100 | 3 | - | - | 1 | - | - | - | 3 | - | - | 9 | 78 | HIF, CMT, SDRAM, PCMCIA | BP-176V |
| | 7606 | HD6417606BGW100V | - | 4 | 3.0 | 3.6 | 100 | 3 | - | - | 1 | - | - | - | 3 | - | - | 9 | 78 | HIF, CMT, SDRAM, PCMCIA | BP-176V |
| SH-Tiny | 7125 | R5F71242D50FPV | 64 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 4 | 31 | MTU2, CMT | FP-48F |
| | 7125 | R5F71242N50FPV | 64 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 4 | 31 | MTU2, CMT | FP-48F |
| | 7125 | R5F71243D50FPV | 128 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 4 | 31 | MTU2, CMT | FP-48F |
| | 7125 | R5F71243N50FPV | 128 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 4 | 31 | MTU2, CMT | FP-48F |
| | 7125 | R5F71252D50FAV | 64 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64A |
| | 7125 | R5F71252N50FAV | 64 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64A |
| | 7125 | R5F71252D50FPV | 64 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64K |
| | 7125 | R5F71252N50FPV | 64 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64K |
| | 7125 | R5F71253D50FAV | 128 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64A |
| | 7125 | R5F71253N50FAV | 128 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64A |
| | 7125 | R5F71253D50FPV | 128 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64K |
| | 7125 | R5F71253N50FPV | 128 | 8 | 4.5 | 5.5 | 50 | 4 | - | 8 | 1 | - | 8 | - | 3 | - | - | 5 | 45 | MTU2, CMT | FP-64K |
| SH2-DSP | 7065 | HD64F7065SV | 256 | 8 | 3.0 | 3.6 | 60 | 4 | - | 6 | 1 | - | 8 | 2 | 3 | - | 4 | 9 | 118 | MMT, DSP, CMT, TPU | FP-176 |
| SH-2A | 7206 | R5S72060W200FPV | - | 128 | 1.15 | 1.35 | 200 | 3 | - | 9 | 1 | 1 | 8 | 2 | 4 | - | 8 | 17 | 79 | MTU2, MTU2S, CMT, SDRAM | FP-176CV |
| | 7211 | R5F72115D160FPV | 512 | 32 | 3.0 | 3.6 | 160 | 3 | - | 2 | 1 | 9 | 8 | 2 | 4 | - | 8 | 9 | 75 | MTU2, MTU2S, CMT, I²C | FP-144L |
| | 7203 | R5S72030W200FP | - | 32 | 1.15 | 1.35 | 80 | 3 | 2 | 6 | 1 | - | 8 | 2 | 8 | - | 8 | 17 | 82 | FPU, LCDC, USB, I²C, SSI, MTU2, CAN, FLCTL, SDRAM | FP-240V |
| | 7261 | R5S72611C120FPV | - | 32 | 1.15 | 1.35 | 120 | 3 | 2 | 6 | 1 | - | 8 | 2 | 8 | - | 8 | 17 | 123 | MTU2, CAN, I²C, FPU, SSI, SDRAM | FP-176EV |
| | 7261 | R5S72611P80FPV | - | 32 | 1.15 | 1.35 | 80 | 3 | 2 | 6 | 1 | - | 8 | 2 | 8 | - | 8 | 17 | 123 | | FP-176EV |
| | 7261 | R5S72611C120FPV | - | 32 | 1.15 | 1.35 | 120 | 3 | 2 | 6 | 1 | - | 8 | 2 | 8 | - | 8 | 17 | 123 | | FP-176EV |

## SH-Ether Series Line-up



# SH-Ether CPUs for networking and OA applications

## Features

- Built-in 10/100Mbps or 10/100/1000Mbps Ethernet MAC with up to 8KB FIFO for better network efficiency and dedicated DMAC for efficient data transfer
- Easy connectivity via built-in peripherals such as USB function controllers
- Large-size on-chip memory: Up to 16KB RAM and 32/32KB instruction/data cache for higher performance
- Widely supported by third parties and Renesas; product-ready platforms, schematics, software and middleware available
- On-chip hardware support for debugging
- Clever power management
  - Three power-down modes for lower power consumption
  - Clock gearing enables clock to be changed on the fly
  - On-chip hardware support for debugging
- Highly-integrated RISC CPUs in compact micro-BGA and QFP packages reduce board space and system cost

## Applications

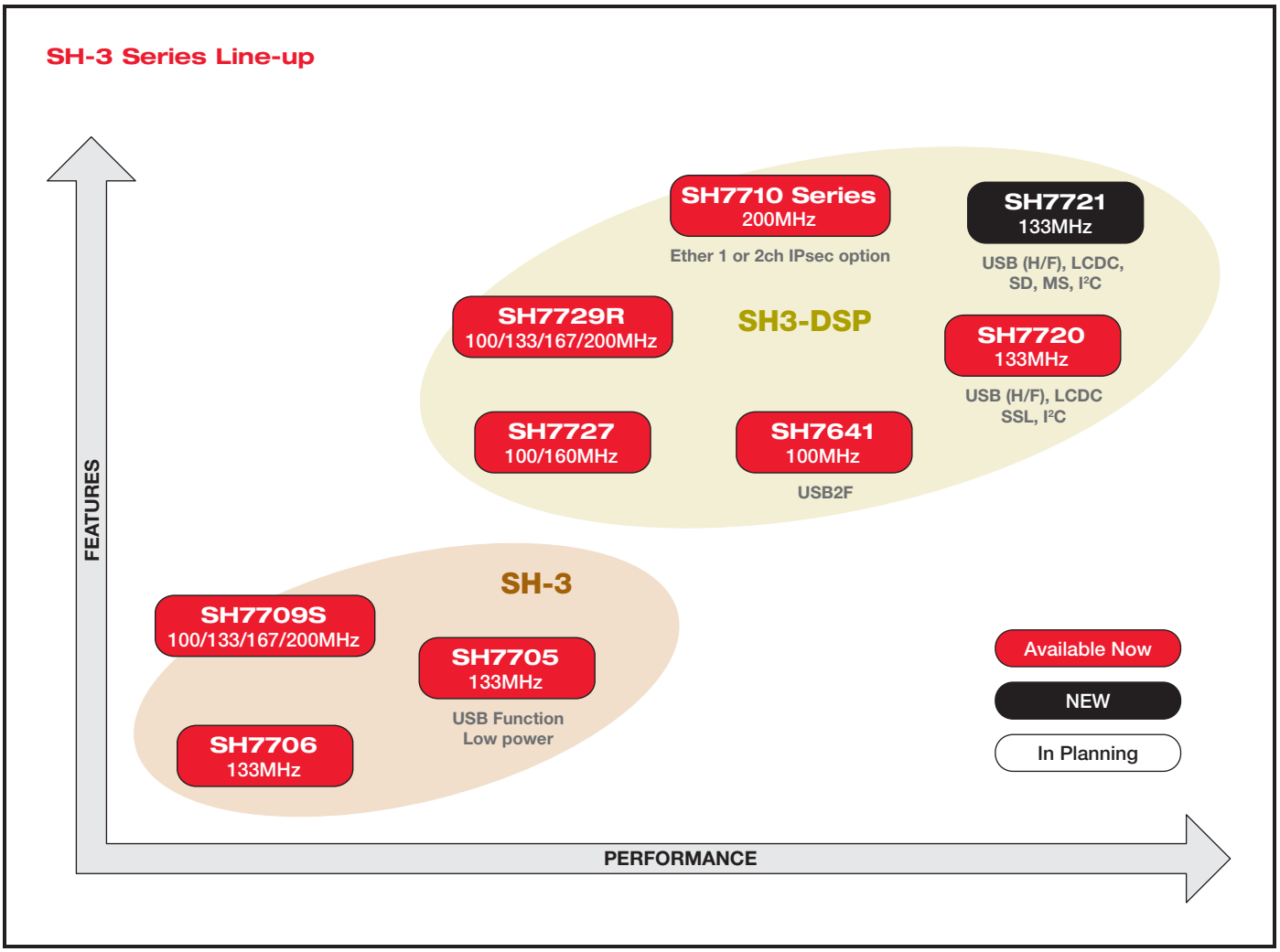
**Network/Communication:**
Network printers, network security cameras, networked factory automation terminals, routers, cable modems, home gateways, etc.

**Office Appliances:**
Printers, scanners, postage meters

**Consumer:**
DVD recorders, HDD recorders, digital home appliances

## SH-Ether Series Selector Guide

| Series | Group | Device Number | RAM (Kbytes) | Vcc min | Vcc max | max MHz @ Vcc max | Watchdog Timer | A/D 10-bit resolution | D/A 8-bit resolution | Serial (Sync/Async) | SSU (SPI Compatible) | DMA Channels | External Interrupts | GPIO | Special Features | Package Code |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SH2-DSP | 7616 | HD6417616ARFV | 8 | 3.0 | 3.6 | 62.5 | 1 | - | - | 5 | - | 2 | 5 | 30 | DSP, Ether MAC, SDRAM | FP-208C |
| SH-2 | 7618 | HD6417618RBGN100V | 4 | 3.0 | 3.6 | 100 | 1 | - | - | 3 | - | - | 9 | 78 | HIF, Ether MAC, PCMCIA, SDRAM | BP-176V |
| | 7618 | HD6417618RBGN100V | 4 | 3.0 | 3.6 | 100 | 1 | - | - | 3 | - | - | 9 | 78 | HIF, Ether MAC, PCMCIA, SDRAM | BP-176V |
| | 7618 | HD6417618RBGW100V | 4 | 3.0 | 3.6 | 100 | 1 | - | - | 3 | - | - | 9 | 78 | HIF, Ether MAC, PCMCIA, SDRAM | BP-176V |
| | 7619 | R4S76190B125BGV | 16 | 3.0 | 3.6 | 125 | 1 | - | - | 4 | - | 4 | 9 | 78 | HIF, Ether MAC PHY, PCMCIA, SDRAM | BP-176V |
| | 7619 | R4S76190N125BGV | 16 | 3.0 | 3.6 | 125 | 1 | - | - | 4 | - | 4 | 9 | 78 | HIF, Ether MAC PHY, PCMCIA, SDRAM | BP-176V |
| | 7619 | R4S76190W125BGV | 16 | 3.0 | 3.6 | 125 | 1 | - | - | 4 | - | 4 | 9 | 78 | HIF, Ether MAC PHY, PCMCIA, SDRAM | BP-176V |
| | 7650 | R4S76500B133BG | 16 | 3.0 | 3.6 | 133 | 1 | - | - | 2 | - | 4 | - | - | HIF, Ether MAC, PCI, PCMCIA, SDRAM | BP-336V |
| SH3-DSP | 7710 | HD6417710BPV | 16 | 1.4 | 1.6 | 200 | 1 | - | - | 4 | - | 6 | 7 | 24 | Dual Ether MAC, IPsec, PCMCIA, SDRAM | BP-256HV |
| | 7710 | HD6417710FV | 16 | 1.4 | 1.6 | 200 | 1 | - | - | 4 | - | 6 | 7 | 24 | Dual Ether MAC, IPsec, PCMCIA, SDRAM | FP-256GV |
| | 7712 | HD6417712BPV | 16 | 1.4 | 1.6 | 200 | 1 | - | - | 4 | - | 6 | 7 | 24 | Dual Ether MAC, PCMCIA, SDRAM | BP-256HV |
| | 7712 | HD6417712FV | 16 | 1.4 | 1.6 | 200 | 1 | - | - | 4 | - | 6 | 7 | 24 | Dual Ether MAC, PCMCIA, SDRAM | FP-256GV |
| | 7713 | HD6417713BPV | 16 | 1.4 | 1.6 | 200 | 1 | - | - | 4 | - | 6 | 7 | 24 | Ether MAC, PCMCIA, SDRAM | BP-256HV |
| | 7713 | HD6417713FV | 16 | 1.4 | 1.6 | 200 | 1 | - | - | 4 | - | 6 | 7 | 24 | Ether MAC, PCMCIA, SDRAM | FP-256GV |
| SH-4A | 7763 | R5S77630Y-266BGV | 16 | 1.15 | 1.35 | 266 | 1 | 4 | 2 | 3 | 3 | 6 | 5 | 118 | Dual GbE MAC, USB Host & Function, LCDC, PCI, FPU, DDR | BP-449V |
| | 7764 | R5S77640N300BGV | 16 | 1.1 | 1.3 | 324 | 1 | - | - | 3 | - | 6 | 3 | 69 | Ether MAC, High-speed USB Host/Function, LCDC, ATAPI, I²C, SSI, FPU, NAND | BP-404V |




## SH-3 Features

- Highest MIPS/watt and MIPS/$ ratings in the industry
- Easy connectivity with built-in peripherals such as USB host/function controllers
- Highly-integrated RISC MPUs in compact micro-BGA and QFP packages reduce board space and system cost
- Flexible bus structure: Four-bus structure allows simultaneous DMA, CPU and DSP access
- Widely supported by third parties and Renesas; product-ready platforms, schematics, software and middleware available
- SH3-DSP devices have on-chip DSP for applications such as signal processing, video streaming, etc.
- On-chip hardware support for debugging
- Clever power management for longer battery life
  - Ultra-low power appliances, boasting a current consumption of just 1mA per MHz (e.g., SH7705)
  - Three power-down modes are available to lower power consumption
  - Clock gearing enables clock to be changed on the fly

## Applications

**Office Appliances:**
Laser printers, video printers, scanners, bar code scanners, fax machines, TV conference systems

**Industrial:**
Postage meters, industrial control terminals, medical equipment

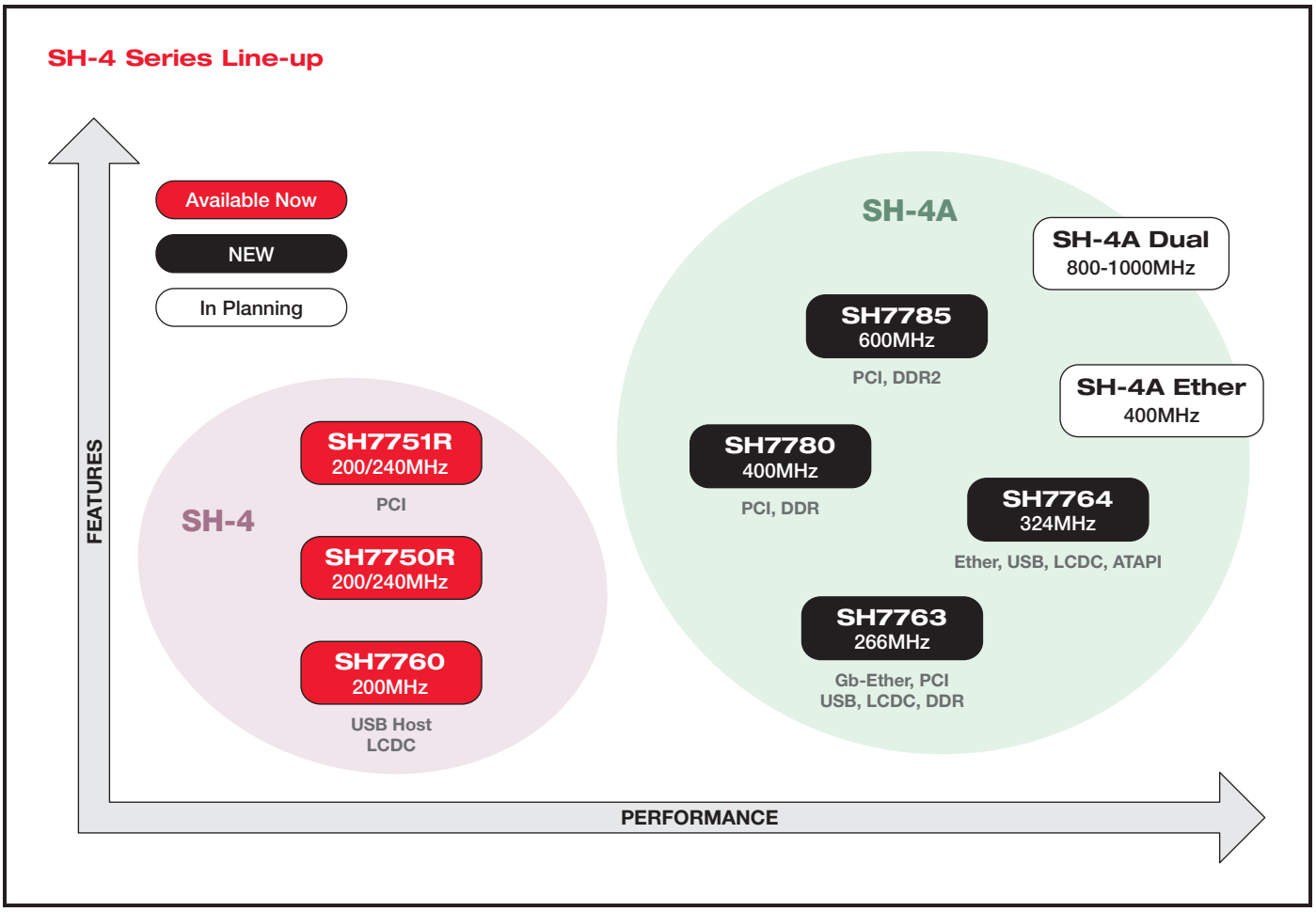
**Consumer:** Digital still cameras, digital video cameras, Web phones

**Network/Communication:**
Low-cost Internet appliances, electronic dictionaries, personal organizers, Handheld PCs, PDAs, point-of-sale terminals, IP telephony, mobile phones, multimedia terminals, portable information devices, web cameras, routers, cable modems

# Up to 200MHz, excellent MIPS/$ for very integrated applications

## SH-3 Series Selector Guide

| Series | Group | Device Number | RAM (Kbytes) | Vcc min | Vcc max | max MHz @ Vcc max | Watchdog Timer | A/D 10-bit resolution | D/A 8-bit resolution | Serial (Sync/Async) | DMA Channels | External Interrupts | GPIO | Special Features | Package Code |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SH-3 | 7705 | HD6417705BP100BV | - | 1.4 | 1.6 | 100 | 1 | 4 | - | 2 | 4 | 7 | 106 | CMT, TPU, USB Function, SDRAM | TBP-208AV |
| | 7705 | HD6417705BP133BV | - | 1.4 | 1.6 | 133 | 1 | 4 | - | 2 | 4 | 7 | 106 | CMT, TPU, USB Function, SDRAM | TBP-208AV |
| | 7705 | HD6417705F100BV | - | 1.4 | 1.6 | 100 | 1 | 4 | - | 2 | 4 | 7 | 106 | CMT, TPU, USB Function, SDRAM | FP-208CV |
| | 7705 | HD6417705F133BV | - | 1.4 | 1.6 | 133 | 1 | 4 | - | 2 | 4 | 7 | 106 | CMT, TPU, USB Function, SDRAM | FP-208CV |
| | 7706 | HD6417706BP133V | - | 1.75 | 2.05 | 133 | 1 | 4 | 2 | 2 | 4 | 7 | 67 | TPU, PCMCIA, SDRAM | TBP-208AV |
| | 7706 | HD6417706F133V | - | 1.75 | 2.05 | 133 | 1 | 4 | 2 | 2 | 4 | 7 | 67 | TPU, PCMCIA, SDRAM | FP-176CV |
| | 7706 | HD6417706F120DV | - | 1.75 | 2.05 | 120 | 1 | 4 | 2 | 2 | 4 | 7 | 67 | TPU, PCMCIA, SDRAM | FP-176CV |
| | 7709S | HD6417709SBP100BV | - | 1.55 | 1.95 | 100 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | BP-240AV |
| | 7709S | HD6417709SF100BV | - | 1.55 | 1.95 | 100 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | FP-208CV |
| | 7709S | HD6417709SBP133BV | - | 1.65 | 2.05 | 133 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | BP-240AV |
| | 7709S | HD6417709SF133BV | - | 1.65 | 2.05 | 133 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | FP-208CV |
| | 7709S | HD6417709SBP167BV | - | 1.75 | 2.05 | 167 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | BP-240AV |
| | 7709S | HD6417709SF167BV | - | 1.75 | 2.05 | 167 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | FP-208CV |
| | 7709S | HD6417709SHF200BV | - | 1.85 | 2.15 | 200 | 1 | 8 | 2 | 3 | 4 | 23 | 96 | TPU, PCMCIA, SDRAM | FP-208EV |
| SH3-DSP | 7641 | HD6417641BP100 | 144 | 1.71 | 1.89 | 100 | 1 | 8 | - | 3 | 4 | 9 | 144 | CMT, USB Function, I²C , SDRAM | BP-256V |
| | 7720 | HD6417720BP133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM | BP-256HV |
| | 7720 | HD6417720BL133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM | BP-256CV |
| | 7720 | HD6417320BP133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM, SD | BP-256HV |
| | 7720 | HD6417320BL133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM, SD | BP-256CV |
| | 7720 | HD6417321BP133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM, MS | BP-256HV |
| | 7720 | HD6417321BL133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM, MS | BP-256CV |
| | 7720 | HD6417330BP133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM, SD, MS | BP-256HV |
| | 7720 | HD6417330BL133CV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SSL, SDRAM, SD, MS | BP-256CV |
| | 7720 | R8A77210C133BGV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM | BP-256HV |
| | 7720 | R8A77210C133BAV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM | BP-256CV |
| | 7720 | R8A77211C133BGV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM, SD | BP-256HV |
| | 7720 | R8A77211C133BAV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM, SD | BP-256CV |
| | 7720 | R8A77212C133BGV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM, MS | BP-256HV |
| | 7720 | R8A77212C133BAV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM, MS | BP-256CV |
| | 7720 | R8A77213C133BGV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM, SD, MS | BP-256HV |
| | 7720 | R8A77213C133BAV | 16 | 1.4 | 1.6 | 133 | 1 | 4 | 2 | 2 | 6 | 7 | 117 | TMU, USB Host & Function, LCDC, PCMCIA, MMC, SDRAM, SD, MS | BP-256CV |
| | 7729R | HD6417729RBP100B | 16 | 1.55 | 1.95 | 100 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | BP-240A |
| | 7729R | HD6417729RF100BV | 16 | 1.55 | 1.95 | 100 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | FP-208CV |
| | 7729R | HD6417729RBP133BV | 16 | 1.65 | 2.05 | 133 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | BP-240AV |
| | 7729R | HD6417729RF133BV | 16 | 1.65 | 2.05 | 133 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | FP-208CV |
| | 7729R | HD6417729RBP167B | 16 | 1.75 | 2.05 | 167 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | BP-240A |
| | 7729R | HD6417729RF167BV | 16 | 1.75 | 2.05 | 167 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | FP-208CV |
| | 7729R | HD6417729RHF200BV | 16 | 1.85 | 2.15 | 200 | 1 | 8 | 2 | 3 | 4 | 7 | 96 | TMU, PCMCIA, SDRAM | FP-208EV |




## Features

- Two-way superscalar support – top performance per MHz
  - Harvard architecture, RISC and FPU instructions executed in parallel
  - Up to 600MHz 32-bit RISC engine @ 1080 MIPS (32-bit registers, 16-bit instructions)
  - Can access four instructions per memory access (64-bit ext. bus)
- Integrated IEEE754-compliant FPU co-processor
  - High-speed single-precision and double-precision operations
  - Can process an impressive seven million polygons per MHz
- Direct connection to SDRAM, DDR-SDRAM, SRAM, Burst ROM, PCMCIA
- Includes DSP/SIMD instruction – true multimedia acceleration
  - FIPR can perform 4-way dot product in a single cycle
  - FTRV can perform a 4-cycle, 4 x 4 matrix-vector multiplication.
- Optimized cache architecture: double size and 4-way associative to reduce cache misses and minimize latency
- Highly-integrated peripherals on device: e.g., SH7763 includes FPU, USB Host and function, built-in LCD controller, Gigabit Ethernet controller, PCI, etc.
- The SH-4 and SH-4A cores feature an advanced power-saving mechanism with built-in power-down modes
- On-chip hardware support for debugging
- Widely supported by third parties and Renesas; product-ready platforms, schematics, software and middleware available
- Investment protection: upward compatibility and long-term product supply and support

## Applications

Networking/Communications: Handheld PCs, point-of-sale devices, Internet appliances, VoIP/webphones, home gateways, routers

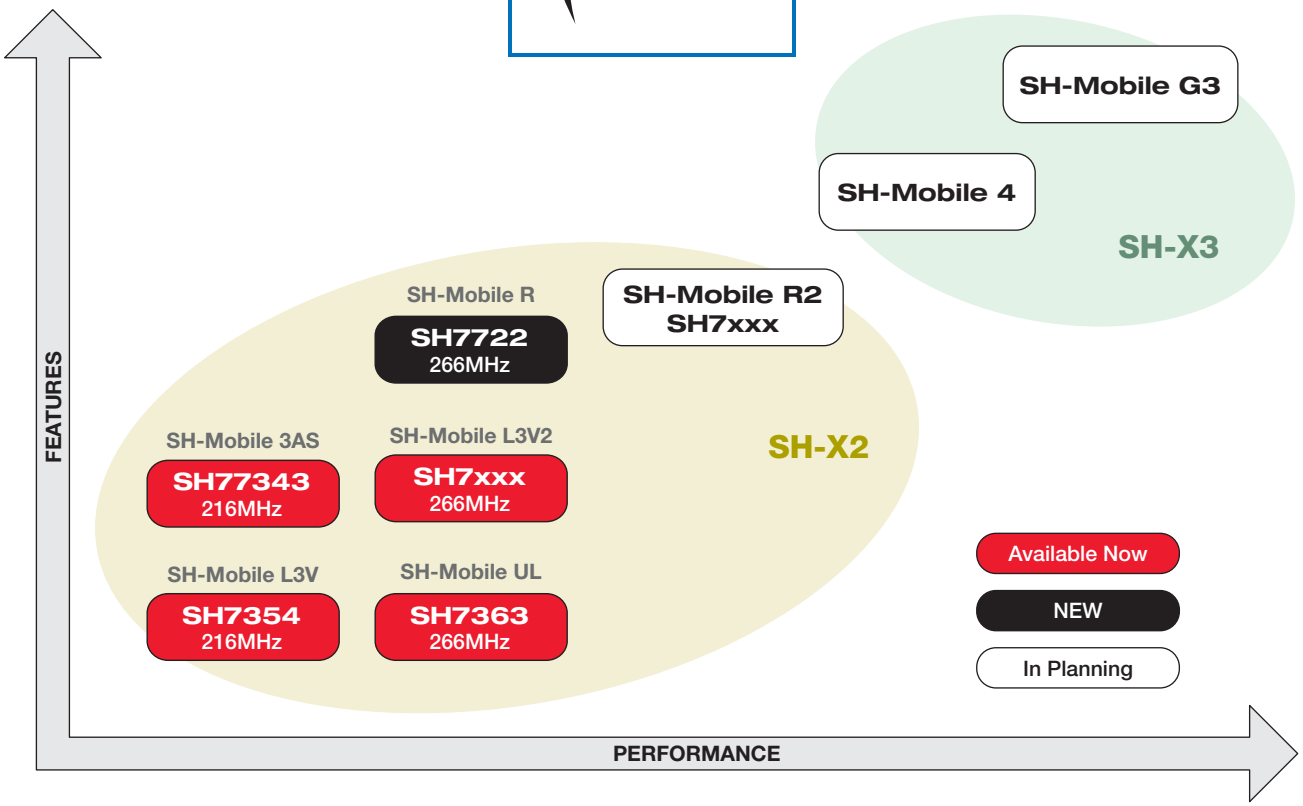
Computing: High-performance multimedia terminals, digital TVs, set-top boxes, game machines, fingerprint detectors, passport readers

# Up to 600MHz, excellent MIPS/$ for very integrated applications

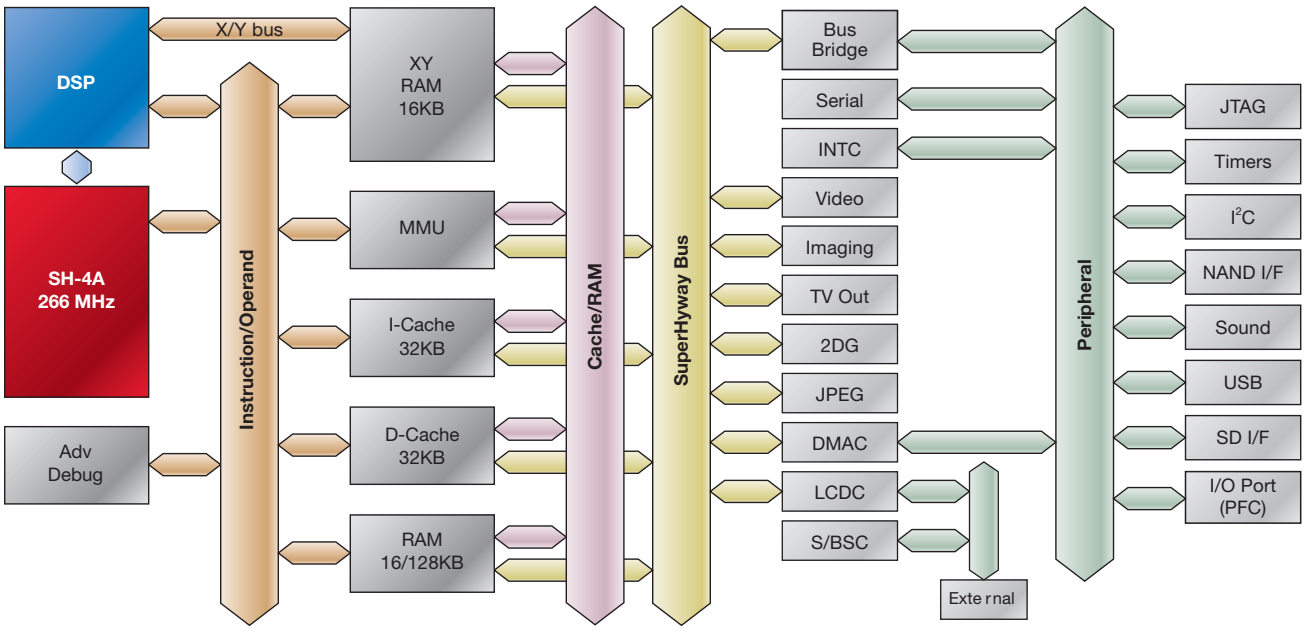
## SH-4 Series Selector Guide

| Series | Group | Device Number | RAM (Kbytes) | Vcc min | Vcc max | max MHz @ Vcc max | Watchdog Timer | A/D 10-bit resolution | D/A 8-bit resolution | Serial (Sync/Async) | DMA Channels | External Interrupts | GPIO | Special Features | Package Code |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SH-4 | 7750R | HD6417750RBP200V | - | 1.35 | 1.6 | 200 | 1 | - | - | 2 | 8 | 5 | 20 | TMU, PCMCIA, FPU, SDRAM | BP-256AV |
| | 7750R | HD6417750RF200V | - | 1.35 | 1.6 | 200 | 1 | - | - | 2 | 8 | 5 | 20 | TMU, PCMCIA, FPU, SDRAM | FP-208EV |
| | 7750R | HD6417750RBP240V | - | 1.4 | 1.6 | 240 | 1 | - | - | 2 | 8 | 5 | 20 | TMU, PCMCIA, FPU, SDRAM | BP-256AV |
| | 7750R | HD6417750RF240V | - | 1.4 | 1.6 | 240 | 1 | - | - | 2 | 8 | 5 | 20 | TMU, PCMCIA, FPU, SDRAM | FP-208EV |
| | 7751R | HD6417751RBP200V | - | 1.35 | 1.6 | 200 | 1 | - | - | 2 | 8 | 5 | 32 | TMU, PCMCIA, FPU, PCI, SDRAM | BP-256AV |
| | 7751R | HD6417751RF200V | - | 1.35 | 1.6 | 200 | 1 | - | - | 2 | 8 | 5 | 32 | TMU, PCMCIA, FPU, PCI, SDRAM | FP-256GV |
| | 7751R | HD6417751RBP240V | - | 1.4 | 1.6 | 240 | 1 | - | - | 2 | 8 | 5 | 32 | TMU, PCMCIA, FPU, PCI, SDRAM | BP-256AV |
| | 7751R | HD6417751RF240V | - | 1.4 | 1.6 | 240 | 1 | - | - | 2 | 8 | 5 | 32 | TMU, PCMCIA, FPU, PCI, SDRAM | FP-256GV |
| | 7760 | HD6417760BP200ADV | - | 1.4 | 1.6 | 200 | 1 | 4 | - | 3 | 8 | 9 | 70 | USB Host, LCDC, AC97, SSI, PCMCIA, FPU, CAN, SDRAM | BP-256FV |
| | 7760 | HD6417760BL200AV | - | 1.4 | 1.6 | 200 | 1 | 4 | - | 3 | 8 | 9 | 70 | USB Host, LCDC, AC97, SSI, PCMCIA, FPU, CAN, SDRAM | BP-256BV |
| | 7760 | HD6417760BL200ADV | - | 1.4 | 1.6 | 200 | 1 | 4 | - | 3 | 8 | 9 | 70 | USB Host, LCDC, AC97, SSI, PCMCIA, FPU, CAN, SDRAM | BP-256BV |
| SH-4A | 7780 | R8A77800ANBGV | 48 | 1.15 | 1.35 | 400 | 1 | - | - | 2 | 12 | 9 | 83 | CMT, TMU, NAND, PCMCIA, MMC, DDR, PCI, FPU, AC97, SSI | BP-449V |
| | 7780 | R8A77800ADBGV | 48 | 1.15 | 1.35 | 400 | 1 | - | - | 2 | 12 | 9 | 83 | CMT, TMU, NAND, PCMCIA, MMC, DDR, PCI, FPU, AC97, SSI | BP-449V |
| | 7781 | R8A77810ANBGV | 48 | 1.15 | 1.35 | 400 | 1 | - | - | 2 | 12 | 9 | 83 | CMT, TMU, NAND, PCMCIA, MMC, DDR, PCI, FPU, AC97, SSI, IPsec | BP-449V |
| | 7781 | R8A77810AHBG | 48 | 1.15 | 1.35 | 400 | 1 | - | - | 2 | 12 | 9 | 83 | CMT, TMU, NAND, PCMCIA, MMC, DDR, PCI, FPU, AC97, SSI, IPsec | BP-449V |
| | 7785 | R8A77850ANBGV | 152 | 1.0 | 1.2 | 600 | 1 | - | - | 6 | 12 | 9 | - | TMU, NAND, PCMCIA, MMC, DDR2, PCI, FPU, AC97, SSI, LCDC | FC-BGA436 |
| | 7785 | R8A77850ADBGV | 152 | 1.0 | 1.2 | 600 | 1 | - | - | 6 | 12 | 9 | - | TMU, NAND, PCMCIA, MMC, DDR2, PCI, FPU, AC97, SSI, LCDC | FC-BGA436 |

## SH-Mobile Series Line-up




## SH-Mobile Series Block Diagram



## Features

- High-performance with low power consumption
  - Superscalar CPU provides ample horsepower at low frequency – 4500 MIPS/W
  - Integral DSP instructions offer flexibility for optimized audio and speech algorithms
- Industry-leading low-power multimedia hardware accelerators
  - H.264, MPEG4, and H.263 video engines with up to D1 resolution offloads CPU, minimizes power consumption, and optimizes visual quality
  - 5Mpixel camera/video input port supports color space conversion, blend, rotate, scale and overlays
  - Realtime JPEG engine speeds up digital imaging operations
  - 2D / 3D graphics engines facilitate smooth user experience
- Up to 24 bpp LCD controller for true color display
- TV output for additional display option
- Integrated sound interface provides rich multimedia experience
- Memory card interface and NAND flash interface offer more expansion options
- Integrated high-speed USB function for PC connectivity

## Applications

**Single-chip multimedia player:**

- Handheld digital TV capability
- Multi-format video
- Multi-format audio
- DRM host
- DVB-H, DMB, ISDB-T, etc.

**VoIP capability for multimedia phones**

**Personal navigation**

**IP camera**

## SH-Mobile Solutions

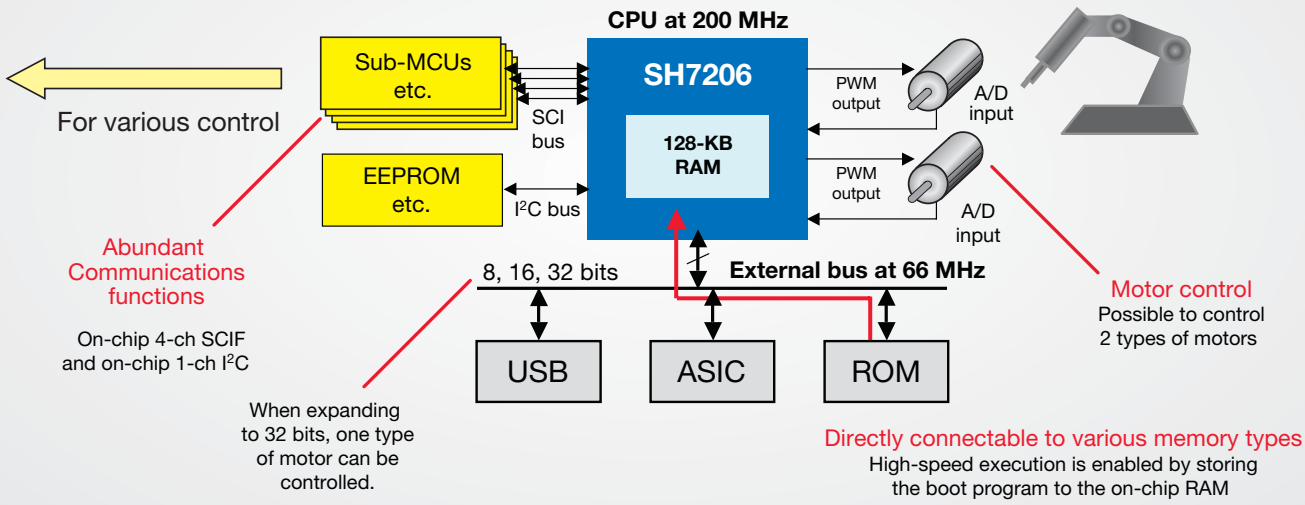
- Development platform
  - SH-Mobile Solution Engine
- RTOS with board support package
  - Embedded Linux BSP
- Multimedia middleware
  - H.264, MPEG4, H.263 video codecs
  - MP3, WMA, AAC, AAC+ audio codecs
  - G.7xx speech codecs, LEC, AEC
  - Media player
- Network stacks
  - TCP/IP
  - RTP
  - SIP
- GUI software
  - QTopia
  - 2D/3D graphics and imaging libraries
- SH-Mobile Consortium
  - Over 200 companies developing middleware, applications, and system designs based on SH-Mobile devices

## SH-Mobile Series Selector Guide

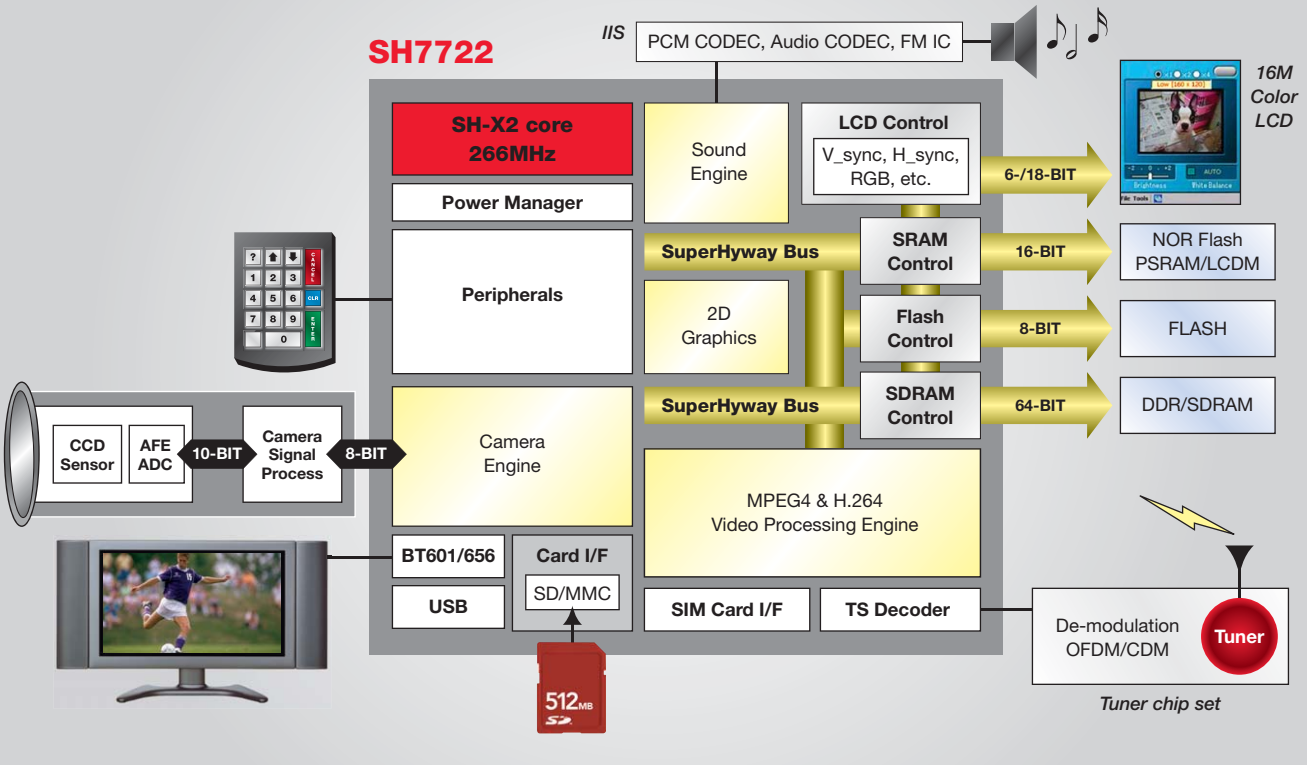
| Group | Device Number | SDRAM (Mbytes) | Vcc min | Vcc max | max MHz @ Vcc max | Watchdog Timer | FLCTL | SDHI | LCD Controller | Serial | I²C | DMA Channels | External Interrupts | GPIO | Special Features | Package Code |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **7343** | R8J73437BGZV | 16 | 1.1 | 1.3 | 216 | 1 | Y | Y | QVGA 24bpp | 7 | 2 | 6 | 9 | 176 | DSP, VPU4, VIO, VOU, JPU, TSIF, SIU, 3DG, USBF, MFI | BP-409V |
| **7354** | R8J73540BGZV | 16 | 1.15 | 1.3 | 216 | 1 | Y | Y | QVGA 18bpp | 3 | 1 | 6 | 6 | 144 | DSP, VPU4, VIO, JPU, TSIF, SIU, MFI | BP-409V |
| **7363** | R8J73630BGV<br>R8J73630BGZV | 16 | 1.15 | 1.3 | 266 | 1 | Y | Y | QVGA 18bpp | 3 | 1 | 6 | 6 | 100 | DSP, VPU5, VIO, VOU, JPU, TSIF, SIU, MFI | BP-409V |
| **7722** | R8A77220AC266BGV | - | 1.15 | 1.3 | 266 | 1 | Y | Y | QVGA 24bpp | 6 | 1 | 6 | 9 | 184 | DSP, VPU4, VIO, VOU, JPU, TSIF, SIU, 2DG | BP-409V |
| | R8A772201AC266BGV | - | 1.15 | 1.3 | 266 | 1 | Y | Y | QVGA 24bpp | 6 | 1 | 6 | 9 | 184 | DSP, VPU4, VIO, VOU, JPU, TSIF, SIU, 2DG, USBF | BP-409V |

## Application Example 1: AC Servo System Configuration Using SH7206 (SH-2 series)

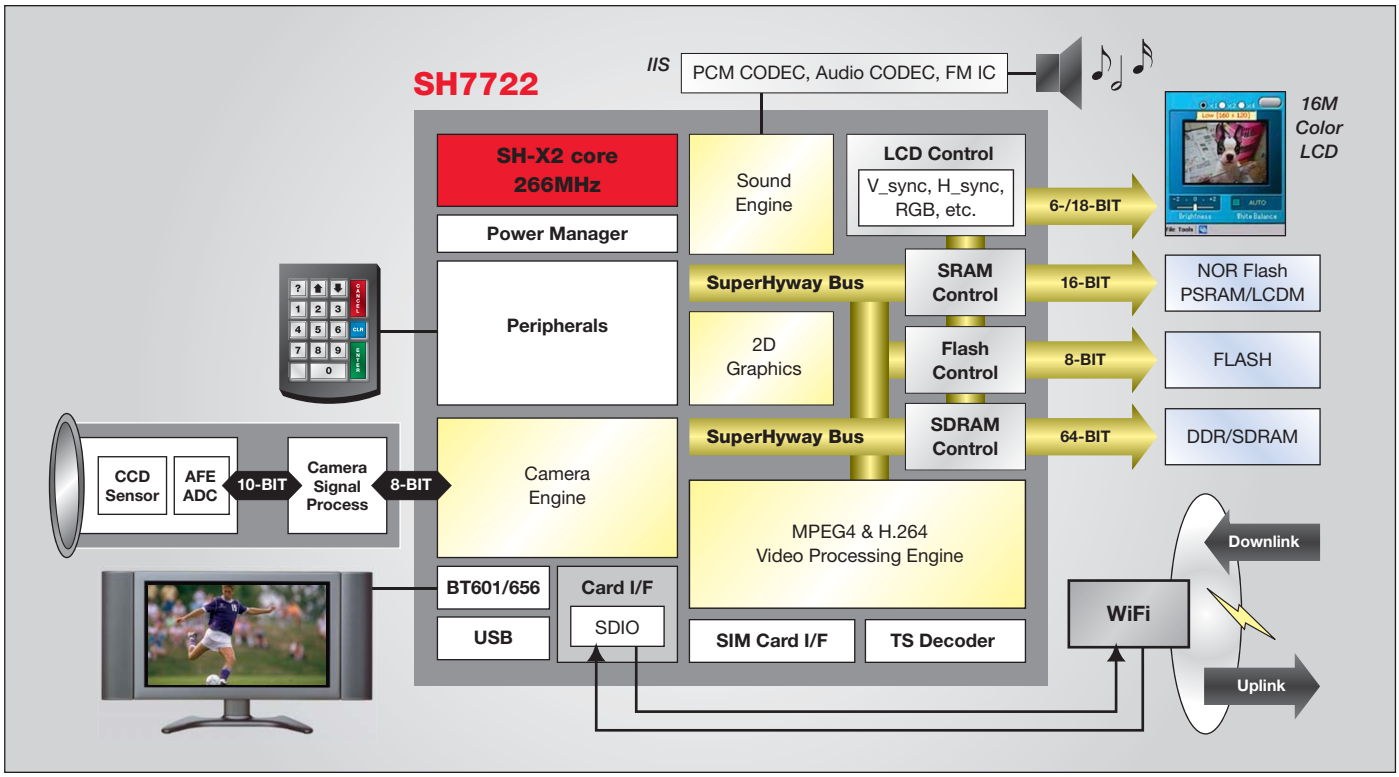
- Achieves maximum CPU performance by having programs resident in internal RAM
- On-chip cache improves performance of externally installed programs
- Abundant functions such as three-phase PWM output timer, 10-bit A/D converter, and more



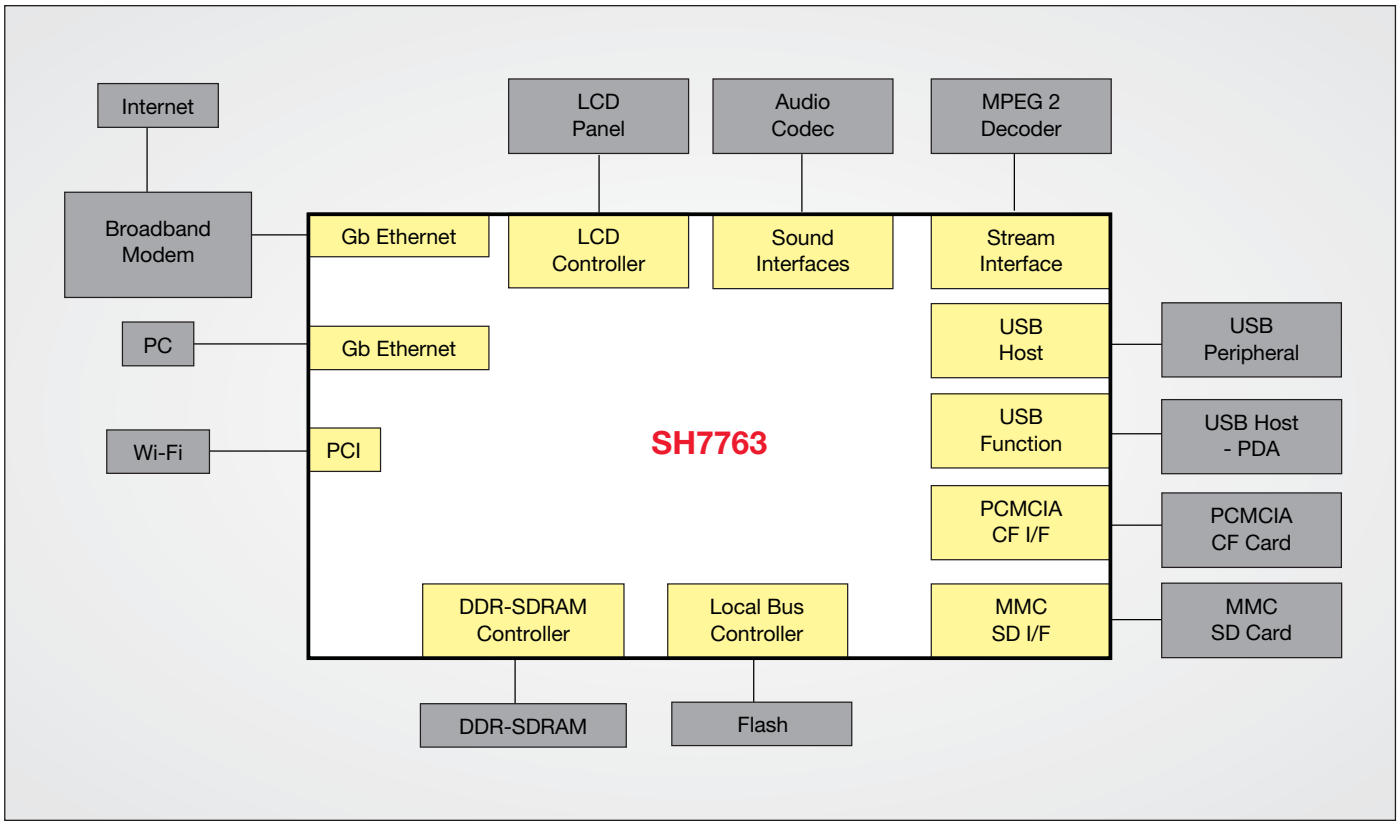

## Application Example 2: Multimedia/Digital TV Player using SH7722 (SH-Mobile series)



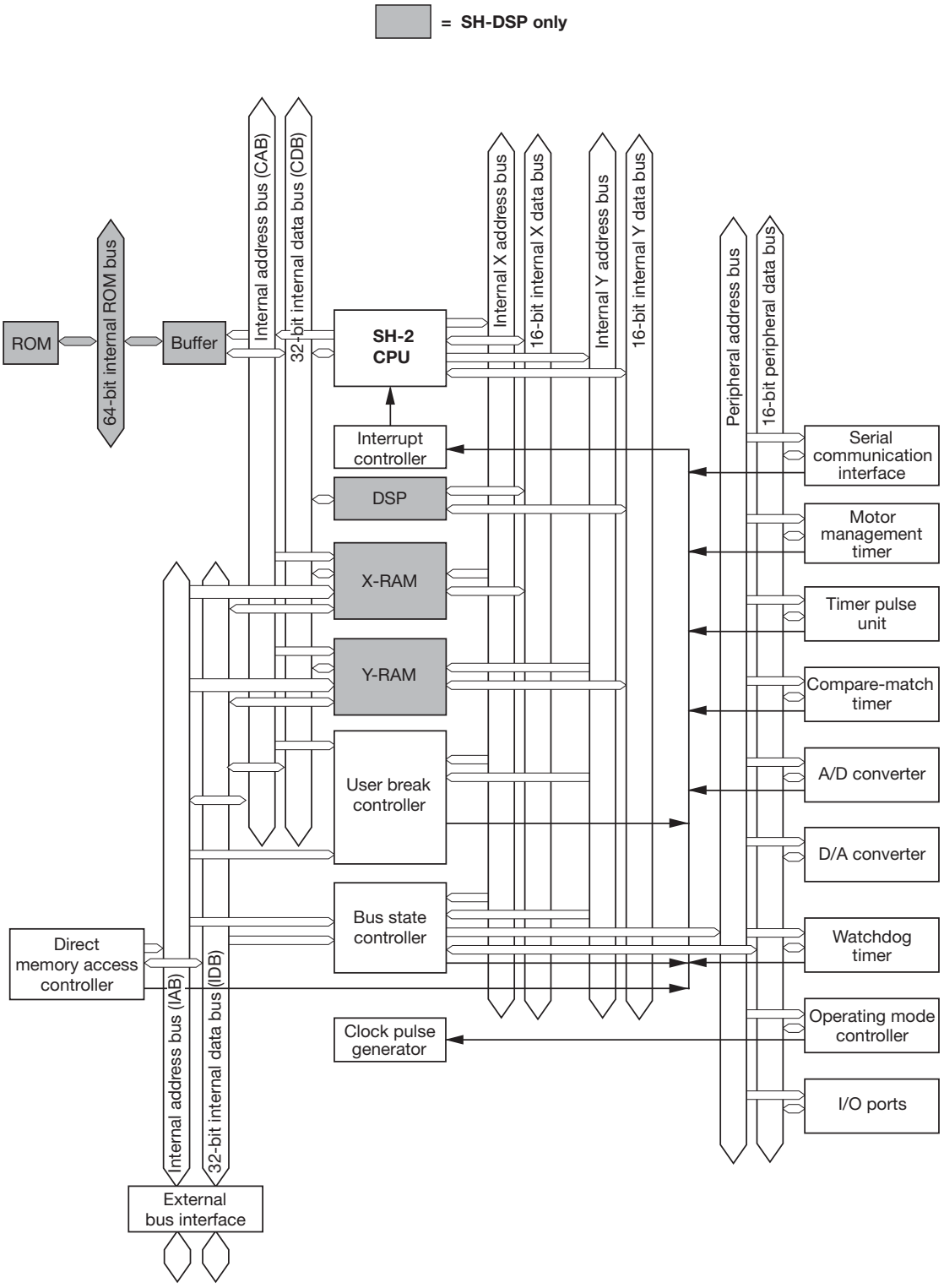
## Application Example 3: Video VoIP System Using SH7722 (SH-Mobile series)




## Application Example 4: Multimedia Gateway Configuration using SH7763 (SH-4 series)



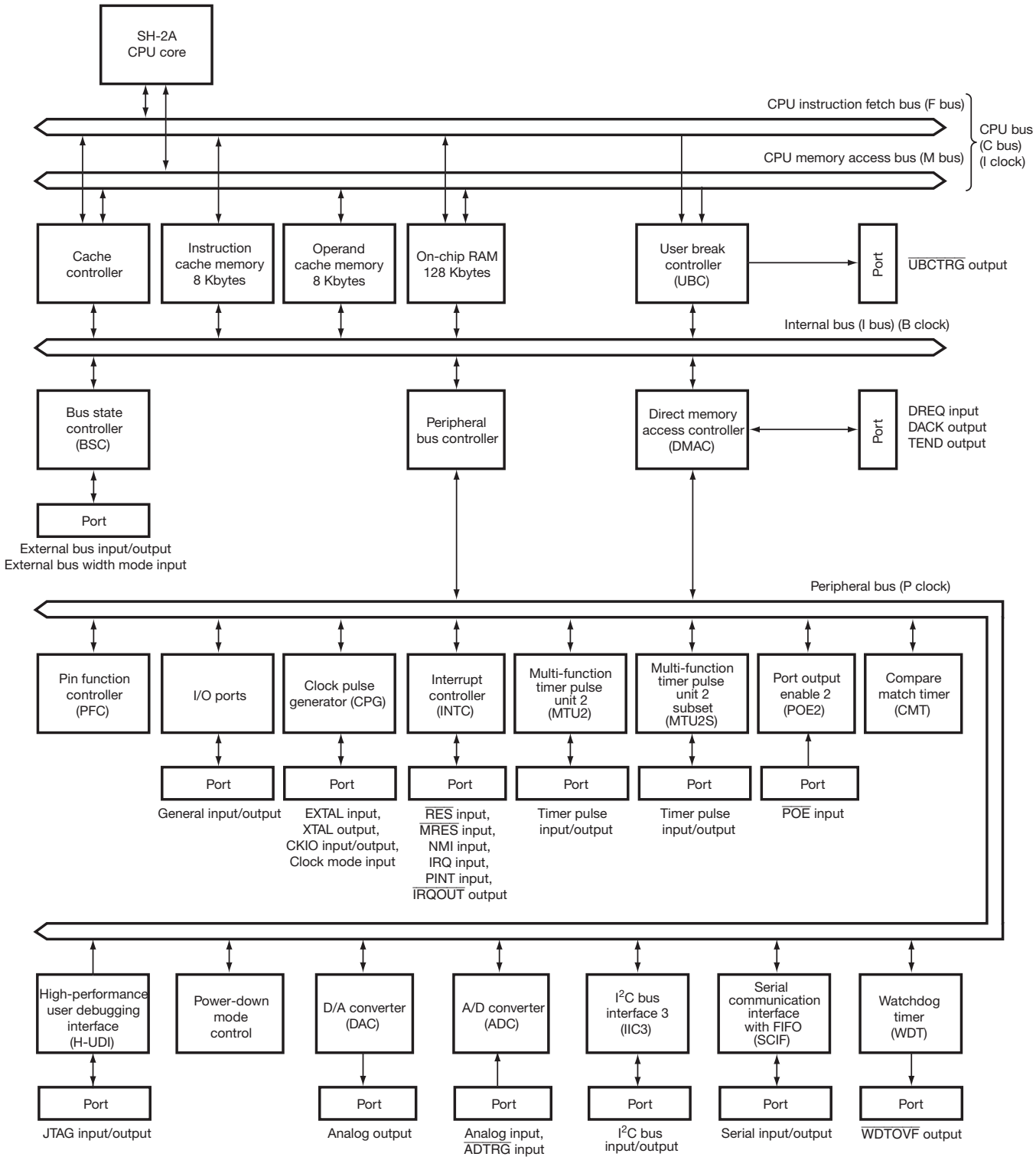
## Appendix A-1: Architecture of SH-2 and SH2-DSP Series




**LEGEND:**

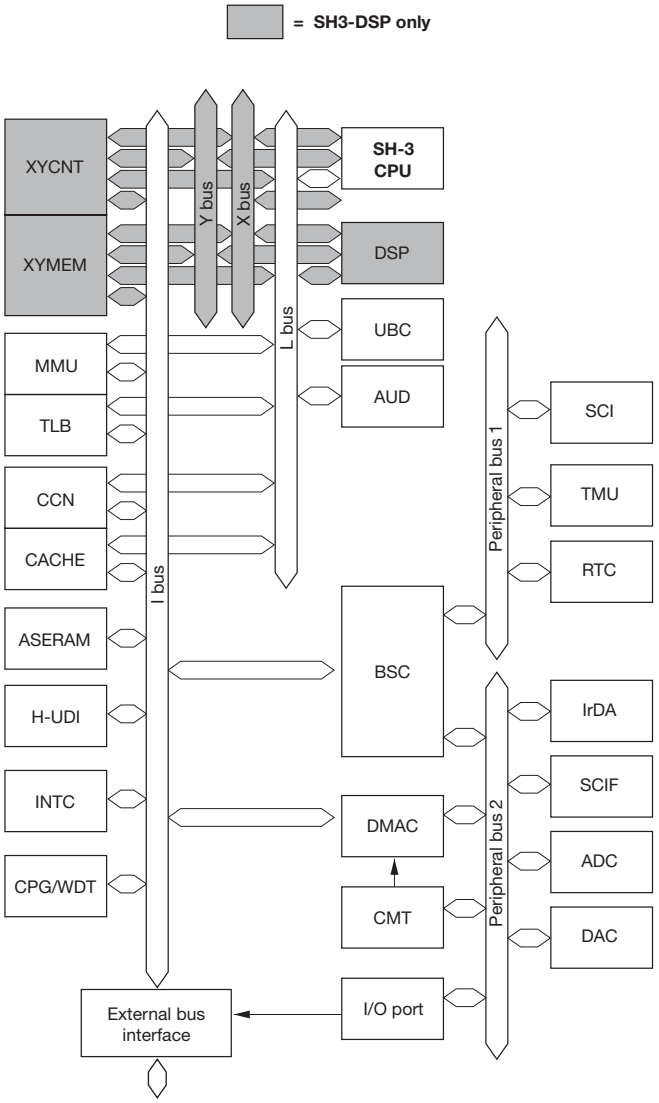
| | | | | | |
|---|---|---|---|---|---|
| CPG | Clock Programmable Generator | MTU | Multifunction Timer Pulse Unit | TIM 2 | 8-Bit Timer 2 |
| ADC | Analog to Digital Converter | CMT | Compare Match Timer | HCAN | Car Automotive Network |
| DAC | Digital to Analog Converter | PWM | Pulse Width Modulater | HCAN2 | Car Automotive Network |
| TPU | 16-Bit Timer Pulse Unit | ATU | Advanced Timer Unit | SCI | Serial Communication Interface |
| WDT | WatchDog Timer | ATU-II | Advanced Timer Unit-II | UDI | User Debug Interface |
| MMT | Motor Management Timer | APC | Advanced Pulse Controller | DTC | Data Transfer Controller |
| | | | | PFC | Pin Function Controller |

## Appendix A-2: Architecture of SH-2A Series



## Appendix A-3: Architecture of SH-3, SH3-DSP, and SH-4 Series

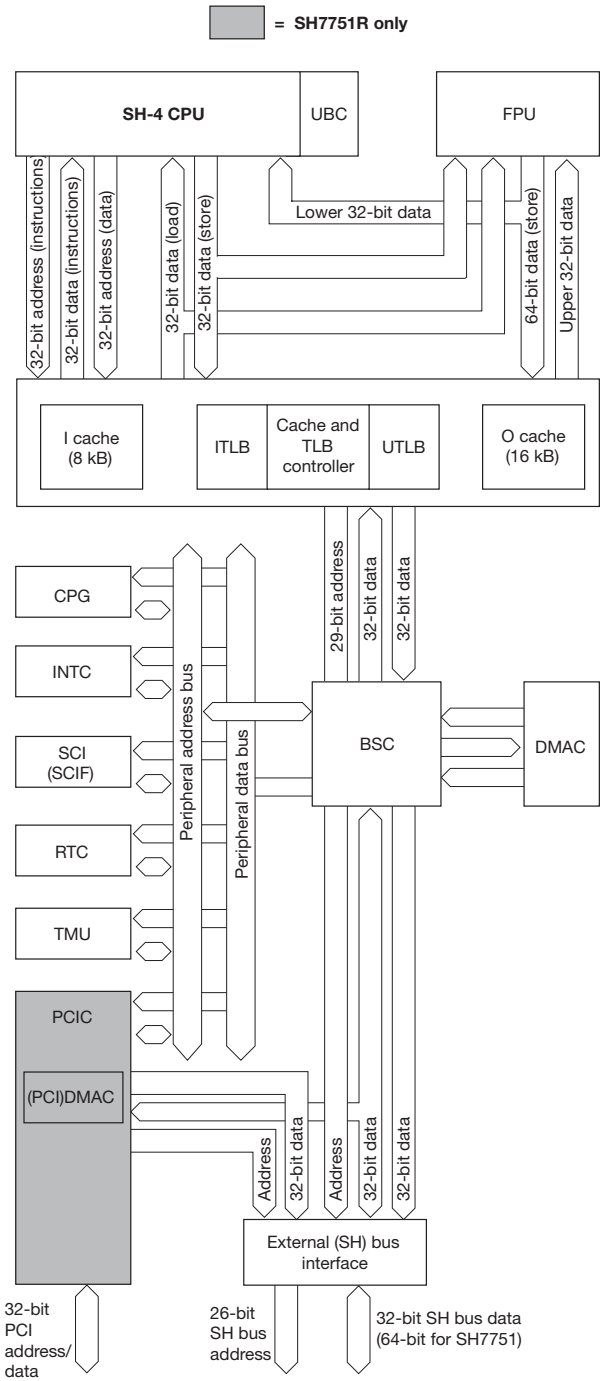
### SH-3, SH3-DSP Architecture




**LEGEND:**

| | |
|---|---|
| ADC: | A/D converter |
| ASERAM: | ASE memory |
| AUD: | Advanced user debugger |
| BSC: | Bus state controller |
| CACHE: | Cache memory |
| CCN: | Cache memory controller |
| CMT: | Compare match timer |
| CPG/WDT: | Clock pulse generator/watchdog timer |
| CPU: | Central processing unit |
| DAC: | D/A converter |
| DMAC: | Direct memory access controller |
| DSP: | Digital signal processor |
| INTC: | Interrupt controller |
| IrDA: | Serial communicatiion interface (with IRDA) |
| MMU: | Memory management unit |
| RTC: | Realtime clock |
| SCI: | Serial communication interface (with smart card interface) |
| SCIF: | Serial communication interface (with FIFO) |
| TLB: | Translation look-aside buffer |
| TMU: | Timer unit |
| UBC: | User break controller |
| UDI: | User debugging interface |
| XYCNT: | X/Y memory controller |
| XYMEM: | X/Y memory |

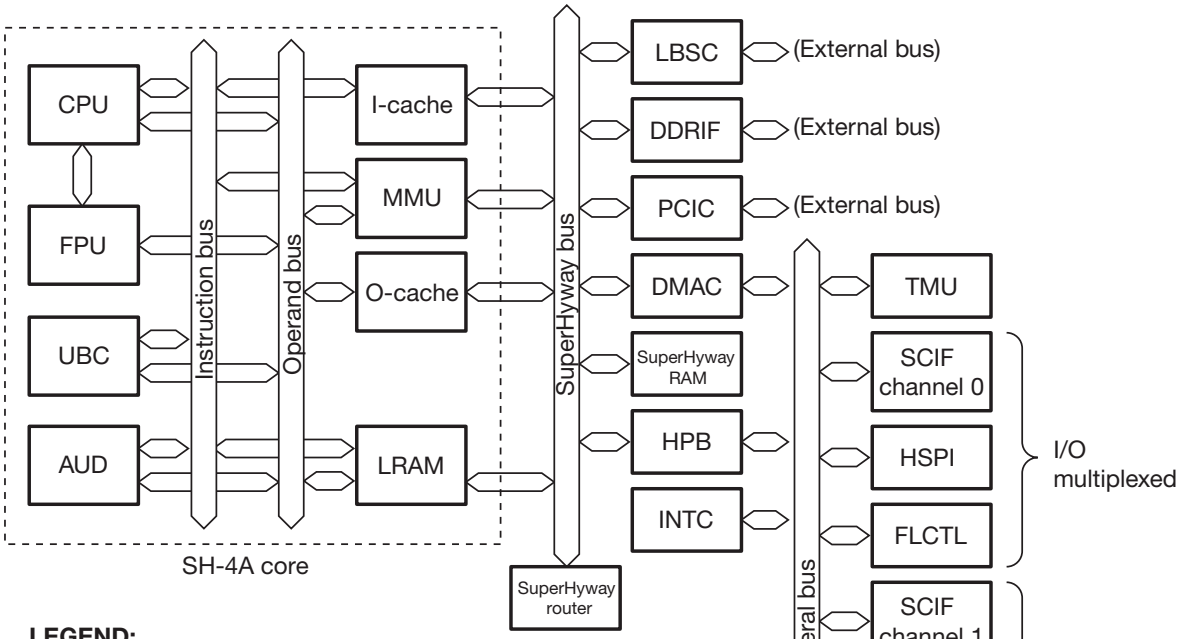
### SH-4 Architecture




**LEGEND:**

| | |
|---|---|
| BSC: | Bus state controller |
| CPG: | Clock pulse generator |
| DMAC: | Direct memory access controller |
| FPU: | Floating-point unit |
| INTC: | Interrupt controller |
| ITLB: | Instruction TLB (translation lookaside buffer) |
| UTLB: | Unified TLB (translation lookaside buffer) |
| RTC: | Realtime clock |
| SCI: | Serial communication interface |
| SCIF: | Serial communication interface with FIFO |
| TMU: | Timer unit |
| UBC: | User break controller |
| PCIC: | PCI bus controller |

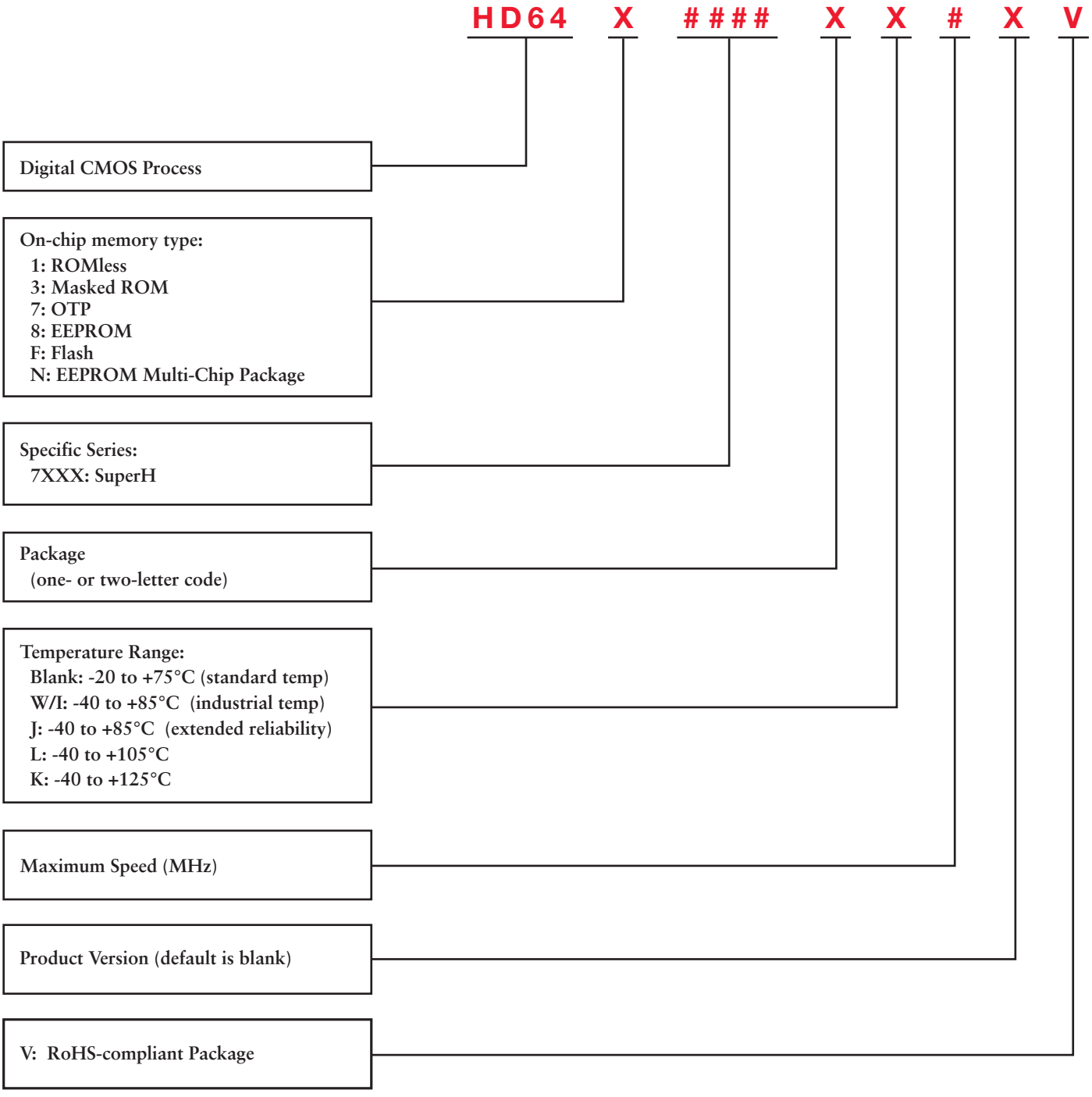
## Appendix A-4: Architecture of SH-4A Series



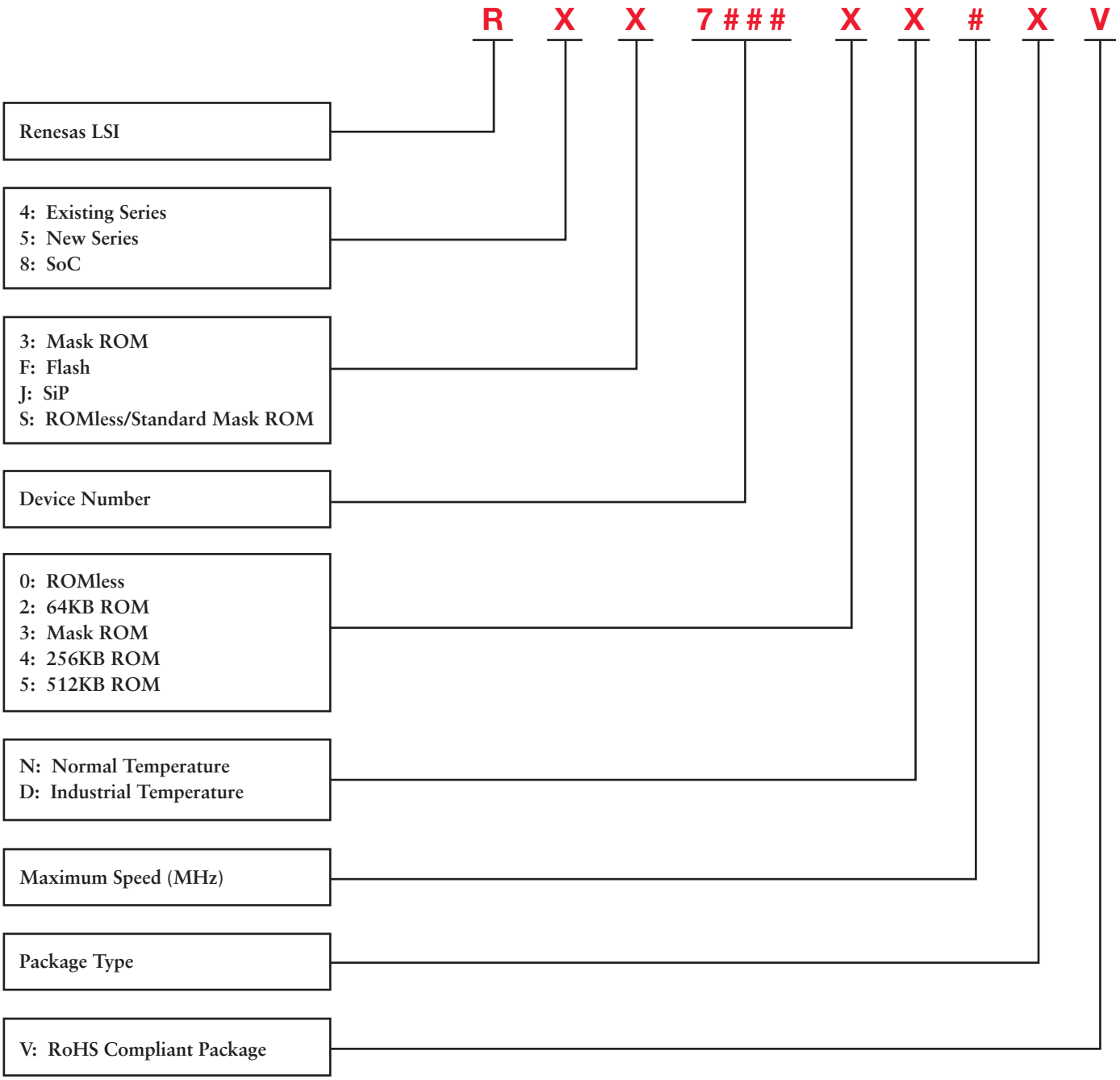

**LEGEND:**

| | |
|---|---|
| AUD: | Advanced user debugger |
| CMT: | Timer/counter |
| CPG: | Clock pulse generator |
| CPU: | Central processing unit |
| DDRIF: | DDR-SDRAM interface |
| DMAC: | Direct memory access controller |
| FLCTL: | NAND flash memory controller |
| FPU: | Floating-point unit |
| GPIO: | General purpose I/O |
| HAC: | Audio codec |
| HPB: | Peripheral bus bridge |
| HSPI: | Serial protocol interface |
| H-UDI: | User debugging interface |
| I-Cache: | Instruction cache |
| INTC: | Interrupt controller |
| LBSC: | Local bus state controller |
| LRAM: | L memory |
| MMCIF: | Multimedia card interface |
| MMU: | Memory management unit |
| O-Cache: | Operand (data) cache |
| PCIC: | PCI controller |
| RTC: | Realtime clock |
| SCIF: | Serial communication interface with FIFO |
| SIOF: | Serial I/O with FIFO |
| SSI: | Serial sound interface |
| SuperHyway RAM: | SuperHyway memory |
| TMU: | Timer unit |
| UBC: | User break controller |
| WDT: | Watchdog timer |

## Appendix B-1: Nomenclature of SuperH Part Numbers (1 of 2)



## Appendix B-2: Nomenclature of SuperH Part Numbers (2 of 2)



## Appendix C: Abbreviations

| | |
|---|---|
| 2DG | 2D Graphics |
| 3DG | 3D Graphics |
| AC97 | AC '97 Audio Interface |
| AUD | Advanced User Debug |
| BSC | Bus State Controller |
| CAN | Controller Area Network |
| CMT | Compare Match Timer |
| DDR | Double Data Rate SDRAM Controller |
| DDR2 | Double Data Rate 2 SDRAM Controller |
| DMA | Direct Memory Access |
| DSP | Digital Signal Processor |
| DTC | Data Transfer Controller |
| Ether MAC | Ethernet Media Access Control |
| Ether PHY | Ethernet Physical Layer |
| FLCTL | NAND Flash Controller |
| FPU | Floating Point Unit |
| GbE MAC | Gigabit Ethernet Media Access Control |
| HIF | Host Interface |
| $I^2C$ | Inter IC Bus |
| IPsec | Internet Protocol Security |
| JPU | JPEG Processing Unit |
| LCDC | LCD Controller |
| MAC | Multiply Accumulate Instruction |

| | |
|---|---|
| MFI | Multi-Function Interface |
| MMC | Multimedia Card |
| MMT | Motor Management Timer |
| MTU | Multi-function Timer pulse Unit |
| MTU2 | Multi-function Timer pulse Unit 2 |
| MTU2S | Multi-function Timer pulse Unit 2S |
| NAND | NAND Flash Controller |
| PCI | PCI Bus Interface |
| PCMCIA | PCMCIA Bus Interface |
| SDHI | Secure Digital Host Interface |
| SDRAM | SDRAM Controller |
| SIU | Sound Interface Unit |
| SSI | Serial Sound Interface |
| SSL | Secure Socket Layer |
| STIF | Stream Interface |
| TMU | Timer Unit |
| TPU | Timer Pulse Unit |
| TSIF | Transport Stream Interface |
| USB Function | Universal Serial Bus Function Interface |
| USB Host | Universal Serial Bus Host Interface |
| VIO | Video Input/Output |
| VOU | Video Output Unit |
| VPU | Video Processing Unit |

## Appendix D: Package Specifications

| Type | Renesas Code | Previous Code | Pin Count | Nominal Body Dimensions (mm) | Lead Pitch (mm) | Thickness (mm) |
|---|---|---|---|---|---|---|
| **QFP (Quad Flat Package)** | PRQP0064GB-A | FP-64A | 64 | 14 x 14 | 0.80 | 3.05 |
| **LQFP (Low-Profile QFP)** | PLQP0048JA-A | FP-48F | 48 | 10 x 10 | 0.65 | 1.70 |
| | PLQP0064KB-A | FP-64K | 64 | 10 x 10 | 0.50 | 1.70 |
| | PLQP0080JA-A | FP-80W | 80 | 14 x 14 | 0.65 | 1.70 |
| | PLQP0100KB-A | FP-100U | 100 | 14 x 14 | 0.50 | 1.70 |
| | PLQP0112JA-A | FP-112E | 112 | 20 x 20 | 0.65 | 1.70 |
| | PLQP0144KA-A | FP-144L | 144 | 20 x 20 | 0.50 | 1.70 |
| | PLQP0176KC-A | FP-176 | 176 | 24 x 24 | 0.50 | 1.70 |
| | PLQP0176KD-A | FP-176CV | 176 | 24 x 24 | 0.50 | 1.70 |
| | PLQP0176KB-A | FP-176E | 176 | 24 x 24 | 0.50 | 1.70 |
| | PLQP0176KB-A | FP-176EV | 176 | 24 x 24 | 0.50 | 1.70 |
| | PLQP0208KA-A | FP-208C | 208 | 28 x 28 | 0.80 | 1.70 |
| | PLQP0208KA-A | FP-208CV | 208 | 28 x 28 | 0.80 | 1.70 |
| **HQFP (Heat-Sinked QFP)** | PRQP0208KE-B | FP-208EV | 208 | 28 x 28 | 0.50 | 3.65 |
| | PRQP0256LA-B | FP-256GV | 256 | 28 x 28 | 0.40 | 3.95 |
| **TQFP (Thin QFP)** | PTQP0100KA-A | TFP-100B | 100 | 14 x 14 | 0.50 | 1.20 |
| **BGA (Ball Grid Array)** | PLBG0256GB-A | BP-256BV | 256 | 17 x 17 | 0.80 | 1.70 |
| | PRBG0256DE-A | BP-256V | 256 | 27 x 27 | 1.27 | 2.50 |
| **FBGA (Fine-Pitch BGA)** | PLBG0281KE-A | BP-281V | 281 | 9 x 11 | 0.50 | 1.40 |
| | TBD | BP-409V | 409 | 12 x 12 | 0.50 | 1.40 |
| | PRBG0436GA-A | BP-436V | 436 | 19 x 19 | 0.80 | TBD |
| | TBD | TBD | 449 | 13 x 13 | 0.50 | TBD |
| | PRBG0449GA-A | BP-449V | 449 | 21 x 21 | 0.80 | 2.00 |
| **LFBGA (Low-Profile Fine-Pitch BGA)** | PLBG0176GA-A | BP-176V | 176 | 13 x 13 | 0.80 | 1.40 |
| | PLBG0240JA-A | BP-240A | 240 | 13 x 13 | 0.65 | 1.40 |
| | PLBG0240JA-A | BP-240AV | 240 | 13 x 13 | 0.65 | 1.40 |
| | PLBG0256KA-A | BP-256CV | 256 | 11 x 11 | 0.50 | 1.40 |
| | PLBG0256FA-A | BP-256FV | 256 | 21 x 21 | 1.00 | 1.70 |
| | PLBG0256GA-A | BP-256HV | 256 | 17 x 17 | 0.80 | 1.40 |
| | PLBG0336GA | BP-336V | 336 | 17 x 17 | 0.80 | 1.40 |

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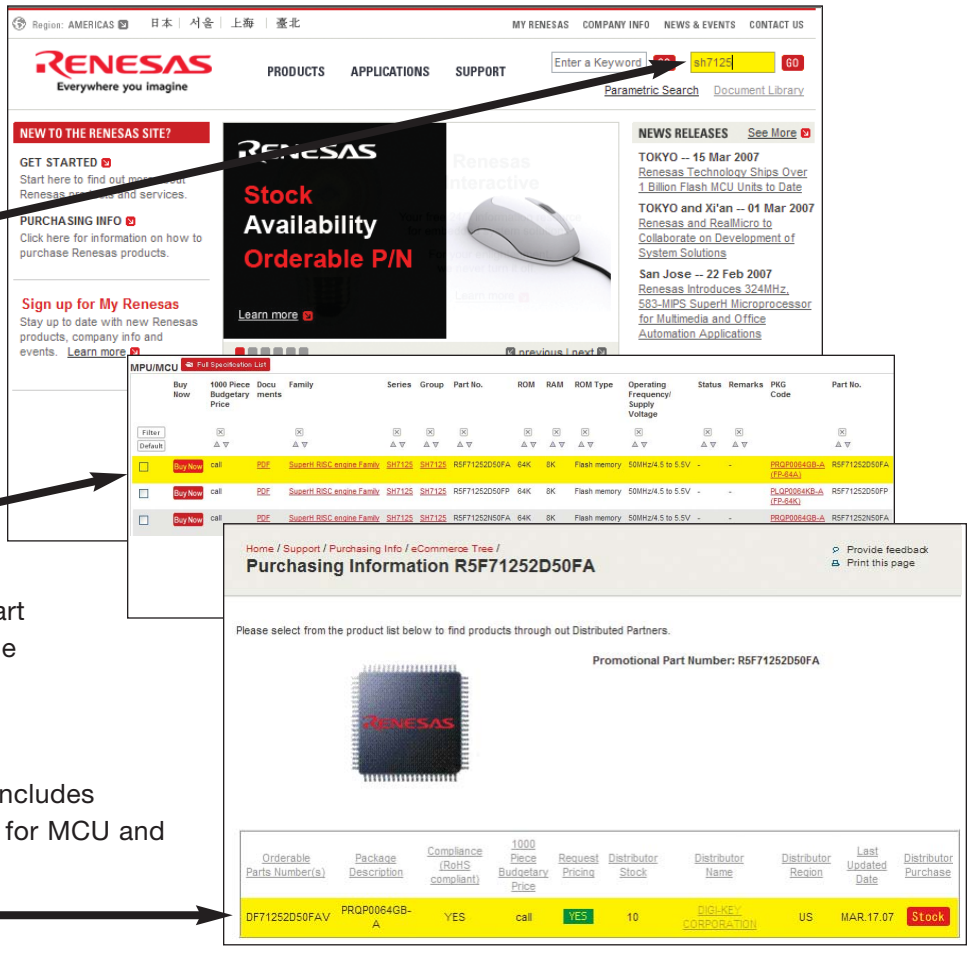


**1** From the Renesas website, in the Part Number search, enter the Series name (example: SH-4A)

**2** Locate the required part number and click on the "Buy Now" button

**3** Purchasing information includes pricing and availability for MCU and related tools

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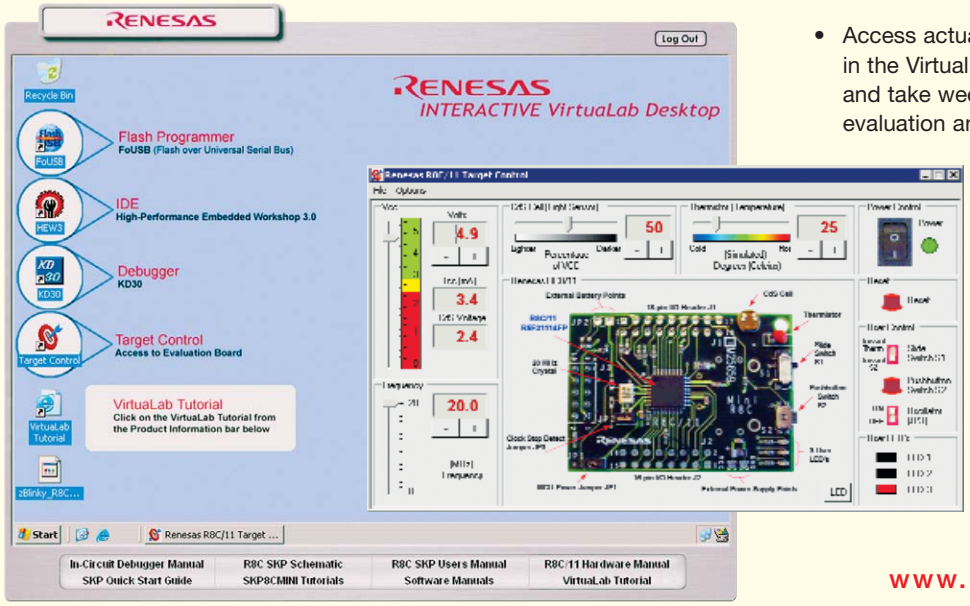


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